

pcb fiducials
TP1 TP2 TP3

INCORRECT CONNECTION
In VS1010 C and D
XRESET should be pulled up to CVDD
Will be corrected in v1.5

UNRELIABLE VALUE
Power button pulse
too short. Use 10 μF
Will be corrected in v1.5

INCORRECT CONNECTION
Crystal load capacitors should
ground to digital ground
Will be corrected in v1.5

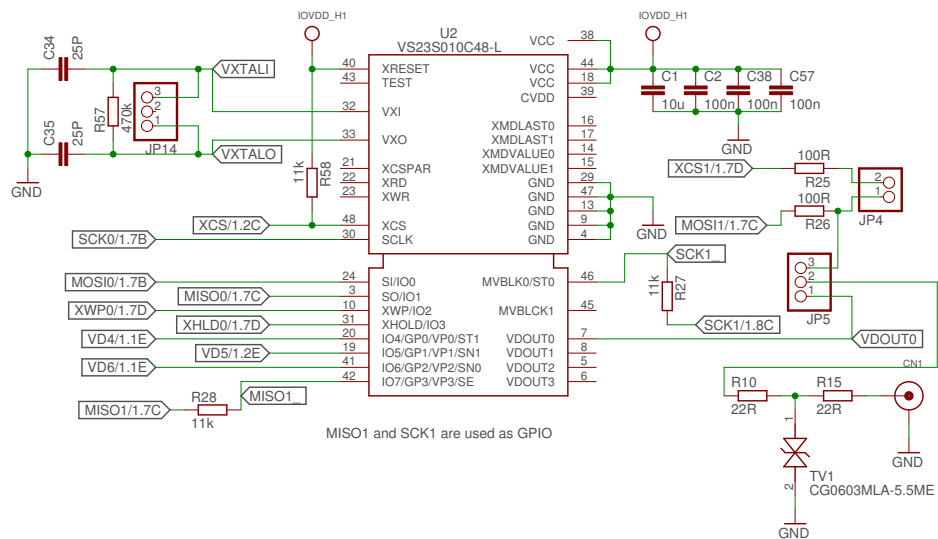
INCORRECT CONNECTION
USB host connector X2
has D+ and D- crossed.
Will be corrected in v1.5

Performance problem: DON'T PUT CAPACITORS ON SPI BUS
Using capacitors to dampen switching oscillation is generally good design.
Here buttons are on SPI bus and capacitors degrade SPI communication

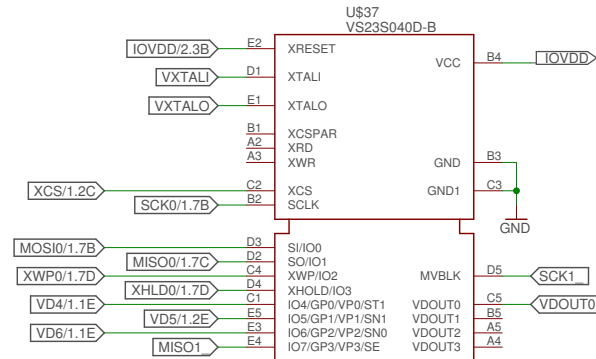
v.1.4.1	- R5, R6, C29, C30 values fixed
	- powerbutton connection fixed
v.1.4.2	- USB host connector error
	- Analog and RAM on separate sheet
v.1.4.3	- XRESET pull up error
	- Crystal ground error
	- Power button capacitor value error
	- Remove button snubbers

Notice! This schematic
matches board version 1.4
VS1010Dev1_43
10.12.2018 13.53
Sheet: 1/3

VS23S010 is populated on VS1010 developer board 1.4. The chip is on the top side.



VS23S040 is not populated on VS1010 developer board 1.4. Footprint is on the bottom side.



Only one of VS23S010 or VS23S040 may be populated.