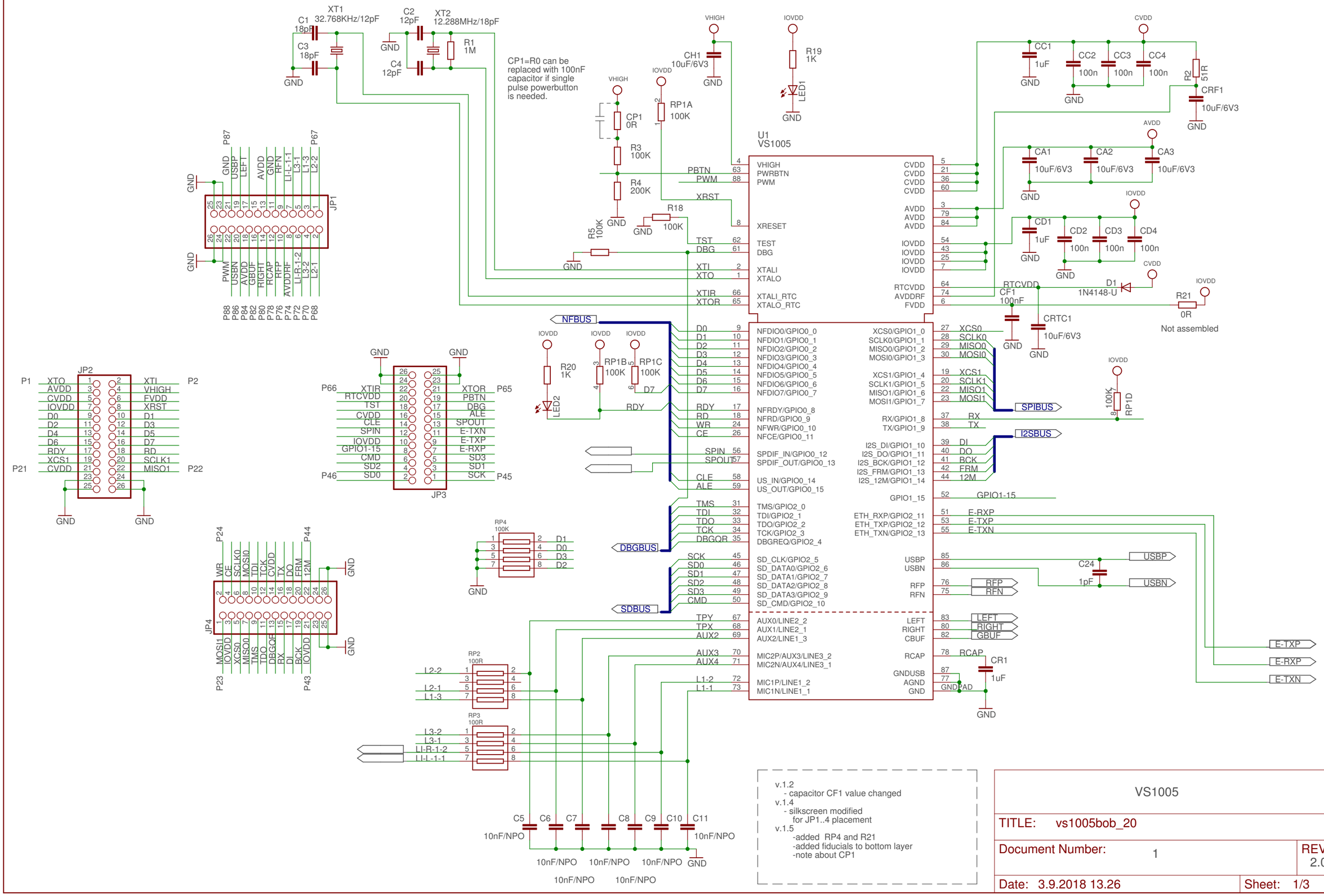
XT1
32.768KHz/12pF
C1
18pF
C3
18pF
GND
C2
12pF
XT2
12.288MHz/18pF
C4
12pF
R1
1M
CP1=R0 can be replaced with 100nF capacitor if single pulse powerbutton is needed.
VHIGH
IOVDD
CH1
10uF/6V3
R19
1K
LED1
CP1
0R
R3
100K
R4
200K
R5
100K
RP1A
100K
R18
100K
U1
VS1005
VHIGH
PWRBTN
PWM
XRST
XRESET
TST
DBG
TEST
DBG
XTI
XTO
XTALI
XTALO
XTIR
XTOR
XTALI_RTC
XTALO_RTC
CVDD
AVDD
IOVDD
RTCVDD
AVDDRF
FVDD
CC1
1uF
CC2
100n
CC3
100n
CC4
100n
R2
51R
CRF1
10uF/6V3
CA1
10uF/6V3
CA2
10uF/6V3
CA3
10uF/6V3
CD1
1uF
CD2
100n
CD3
100n
CD4
100n
D1
1N4148-U
CF1
100nF
CRTC1
10uF/6V3
R21
0R
Not assembled
NFBUS
D0
D1
D2
D3
D4
D5
D6
D7
NFDIO0/GPIO0_0
NFDIO1/GPIO0_1
NFDIO2/GPIO0_2
NFDIO3/GPIO0_3
NFDIO4/GPIO0_4
NFDIO5/GPIO0_5
NFDIO6/GPIO0_6
NFDIO7/GPIO0_7
RDY
RD
WR
CE
NFRDY/GPIO0_8
NFRD/GPIO0_9
NFWR/GPIO0_10
NFCE/GPIO0_11
SPIN
SPOUT
CLE
ALE
SPDIF_IN/GPIO0_12
SPDIF_OUT/GPIO0_13
US_IN/GPIO0_14
US_OUT/GPIO0_15
TMS
TDI
TDO
TCK
DBGQR
DBGBUS
TMS/GPIO2_0
TDI/GPIO2_1
TDO/GPIO2_2
TCK/GPIO2_3
DBGREQ/GPIO2_4
SCK
SD0
SD1
SD2
SD3
CMD
SDBUS
SD_CLK/GPIO2_5
SD_DATA0/GPIO2_6
SD_DATA1/GPIO2_7
SD_DATA2/GPIO2_8
SD_DATA3/GPIO2_9
SD_CMD/GPIO2_10
TPY
TPX
AUX2
AUX3
AUX4
L1-2
L1-1
AUX0/LINE2_2
AUX1/LINE2_1
AUX2/LINE1_3
MIC2P/AUX3/LINE3_2
MIC2N/AUX4/LINE3_1
MIC1P/LINE1_2
MIC1N/LINE1_1
XCS0/GPIO1_0
SCLK0/GPIO1_1
MISO0/GPIO1_2
MOSI0/GPIO1_3
XCS1/GPIO1_4
SCLK1/GPIO1_5
MISO1/GPIO1_6
MOSI1/GPIO1_7
RX/GPIO1_8
TX/GPIO1_9
I2S_DI/GPIO1_10
I2S_DO/GPIO1_11
I2S_BCK/GPIO1_12
I2S_FRM/GPIO1_13
I2S_12M/GPIO1_14
GPIO1_15
ETH_RXP/GPIO2_11
ETH_TXP/GPIO2_12
ETH_TXN/GPIO2_13
USBP
USBN
RFP
RFN
LEFT
RIGHT
CBUF
RCAP
GNDUSB
AGND
GND
GNDPAD
CR1
1uF
SPIBUS
I2SBUS
XCS
SCLK
MISO
MOSI
RX
TX
DI
DO
BCK
FRM
12M
GPIO1-15
E-RXP
E-TXP
E-TXN
C24
1pF
RP1D
100K
JP1
JP2
JP3
JP4
P87
P67
P88
P66
P65
P46
P45
P21
P22
P24
P44
P23
P43
RP2
100R
RP3
100R
RP4
100K
L2-2
L2-1
L1-3
L3-2
L3-1
LI-R-1-2
LI-L-1-1
C5
C6
C7
C8
C9
C10
C11
10nF/NPO
v.1.2
- capacitor CF1 value changed
v.1.4
- silkscreen modified
for JP1..4 placement
v.1.5
-added RP4 and R21
-added fiducials to bottom layer
-note about CP1
VS1005
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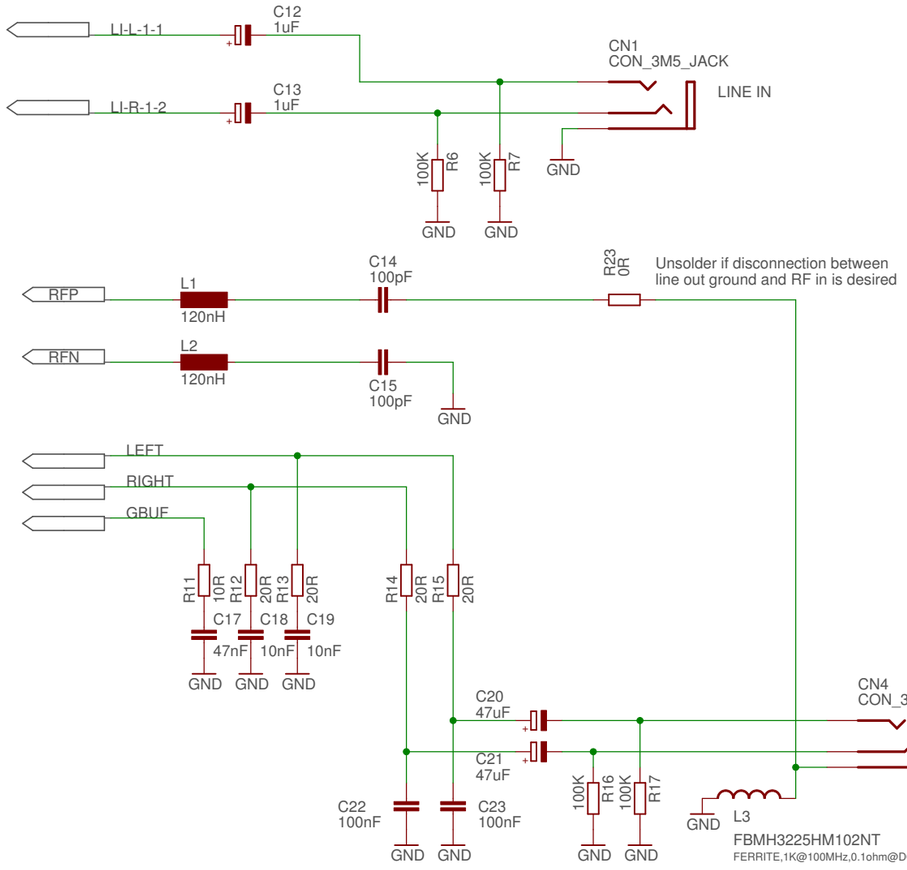

V.1.1
- RTC crystal changed to SMD type
- USB wiring optimized
- GND plane optimized
- RS232 Markings on silkscreen

ANALOG I/O

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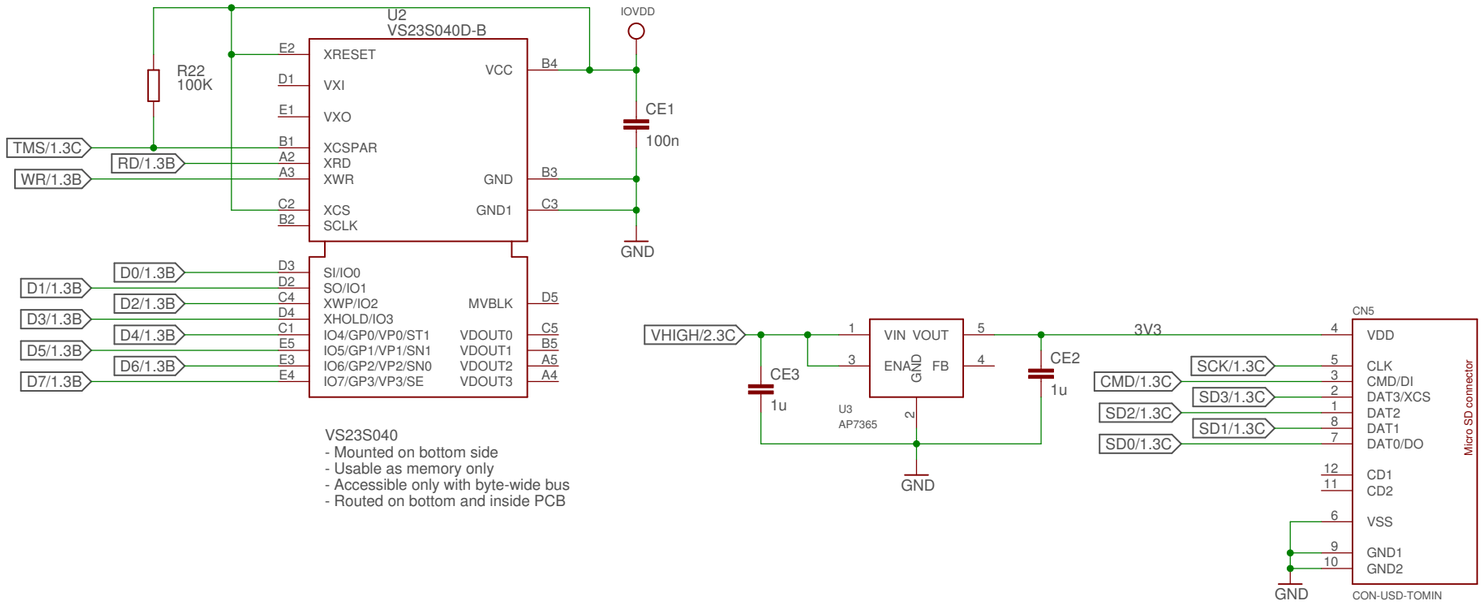

V.2.0
- Added VS23S040
- Added SD card connector and regulator
- C2, C4 30pF -> 12pF
- R23 for separation of line out ground and RF in
- R21 not assembled. IOVDD and FVDD separated

VS23S040

TITLE: vs1005bob_20

Document Number:

REV: v.2.0

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