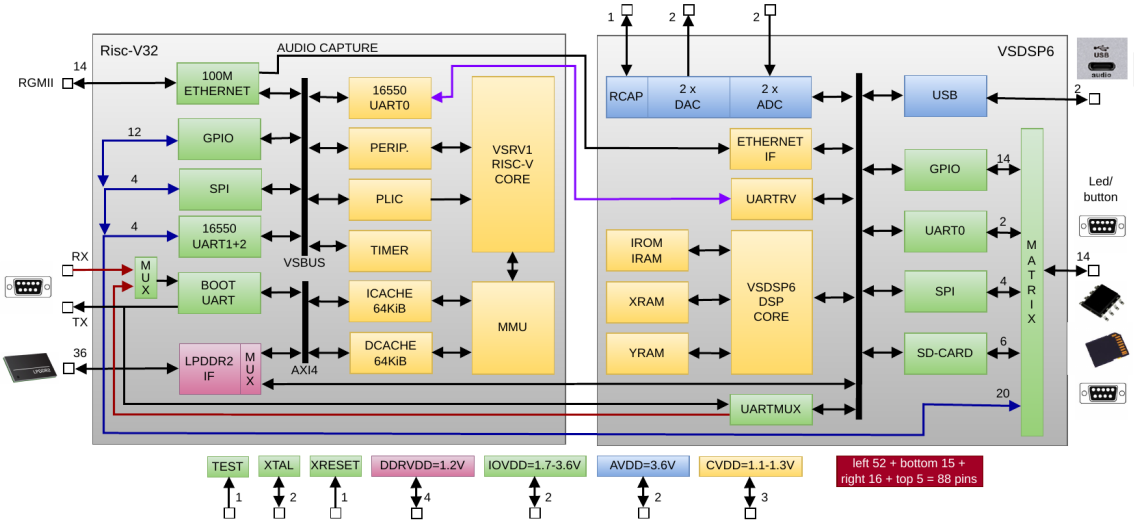
VSRVES01 Datasheet

VSRVES01 - Linux RISC-V + VSDSP^6 Platform IC



Main Features

- Linux-capable RISC-V32 Core
- Proprietary VSDSP^6 core running VSOS
- 100 MHz+ clock
- 6-second boot time until Linux running and DHCP ready (with fast DHCP)
- Analog CD-quality audio Input / Output
- 10/100 Mbit/s RGMII Ethernet interface
- (4+2)xUART, 2xSPI, GPIO
- SD Card and LPDDR interfaces
- Single 12.288 MHz crystal needed
- Compact 0.8mm QFN-88 package

RISC-V Features

- RV32IMS zicsr zifencei core
- Capable of running stock Linux 6.1
- MMU and 2x64 KiB I- and D-Cache

VSDSP^6 Features

- 72/40/16-bit VSDSP^6 core
- 512 KiB fast S-RAM for code and data
- VSOS multitasking Real-Time OS
- Boot time of around 1.5 seconds
- Loads 35 MiB Linux image from SD Card in around 1.5 seconds
- VSOS Shell to run programs

Analog Hardware Features

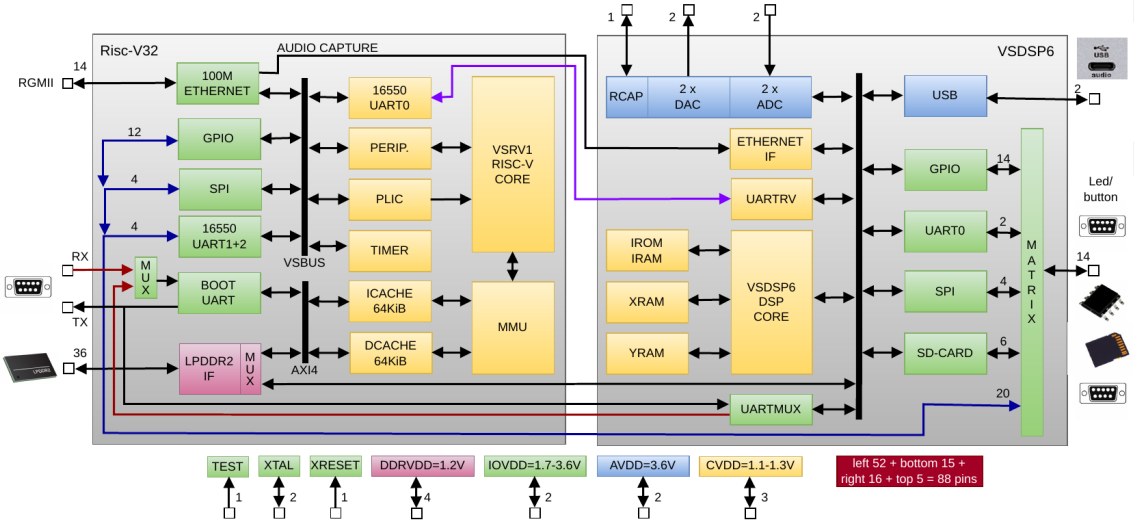
- Two channels of 24-bit audio ADC
- Two 24-bit audio DACs
- Stereo line input / output

Digital Hardware Features

- 16-bit LPDDR2 interface
- 4 external UART interfaces
- 2 internal UARTs
- 2 SPI bus interfaces
- 10/100 Mbit/s RGMII Ethernet interface
- MUX matrix to map I/O pins
- Internal PLLs for various clocks

Applications

- PoE (low-delay) speaker
- Ethernet VoIP
- Network audio player
- Web interface audio player
- Internet radio
- Portable recorders
- MP3 players
- Audio co-processor



System-on-a-Chip Overview

VSRVES01 is a flexible audio platform device. It is built around two cores, one of them RISC-V32, and the other VS_DSP^6. The cores can run software under their respective operating systems simultaneously.

VSRVES01's digital interfaces provide flexible access to external devices in standalone applications. The analog interfaces provide high-quality audio inputs and outputs.

VSRVES01's cold boot time from power-up to a running Linux with network configured is below 7 seconds.

RISC-V Overview

VSRV1 is a 32-bit RISCV ISA CPU core which supports integer (I), multiplication and division (M), CSR instructions (Z), and supervisory (S) extensions (RV32IMS zicsr zifencei).

VSRV1 has an MMU unit and 2x64 KiB caches for Inst/Data memory, adding to its speed.

VSRV1 has been tested and used with stock Linux 6.1. Linux boot time at 111 MHz is less than 3, including starting Ethernet.

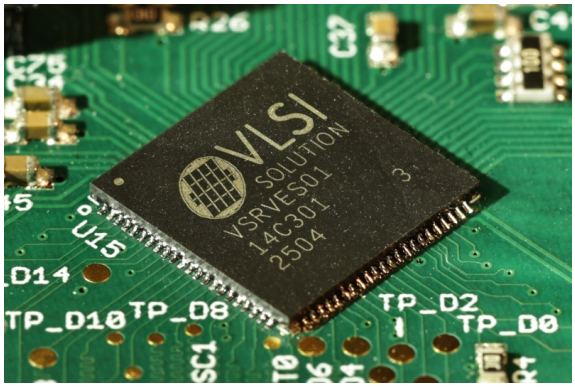
The external memory interface uses an internal AXI4 bus to offer an external LPDDR2 interface. Extrenal LPDDR2 memory is required to run software on VSRV1.

VSDSP^6 Overview

VSDSP^6 is a powerful DSP (Digital Signal Processor) core, running VSOS, VLSI Solution's proprietary DSP-oriented, real-time multitasking operating system.

VSDSP handles amongst other things real-time audio for the VSRVES01, making it much easier for the RISC-V / Linux side to handle audio streams, particularly when low-delay is required. VSDSP can also run several different signal processing algorithms like parametric EQ, AEC, etc.

VSDSP also acts as a boot processor for the system. It can boot its VSOS operating system from SPI Flash in a little over 1 second, then it can load a 35 MiB Linux image, containing a RAM disk, in roughly 1.5 seconds when running at 98 MHz.



Contents

List of Figures

1 Disclaimer

This is an *extremely preliminary* datasheet for engineering samples, still missing lots of information.

While written to be as correct as possible with the information available as of writing the information, here are bound to be errors and omissions, so all properties and figures are very much subject to change.

2 Definitions

ABR Average BitRate. Bitrate of stream may vary locally, but will stay close to a given number when averaged over a longer time.

B Byte, 8 bits.

b Bit.

CBR Constant BitRate. Bitrate of stream will be the same for each compression block.

CBUF Headphone Common Buffer. Outputs DC voltage.

GBUF Same as CBUF.

Ki "Kibi" = 2^{10} = 1,024 (IEC 60027-2).

Mi "Mebi" = 2^{20} = 1,048,576 (IEC 60027-2).

Gi "Gibi" = 2^{30} = 1,073,741,824 (IEC 60027-2).

VBR Variable BitRate. Bitrate will vary depending on the complexity of the source material.

VS_DSP VLSI Solution's DSP core.

VSOS VLSI Solution's Operating System

VSIDE VLSI Solution's Integrated Development Environment.

W Word. In VS_DSP, instruction words are 32 bits and data words are 16 bits wide.

3 Characteristics & Specifications

3.1 Absolute Maximum Ratings

TBD

3.2 Recommended Operating Conditions

TBD

3.3 Analog Characteristics of Audio Outputs

Unless otherwise noted: AVDD=3.6 V, CVDD=1.8 V, IOVDD=2.8 V, V_{ref}=1.6 V, TA=+25°C, XTALI=12 MHz, Internal Clock Multiplier $3.0\times$. DAC tested with full-scale output sinewave, measurement bandwidth 20..20000 Hz, analog output load: LEFT to CBUF 30 Ω, RIGHT to CBUF 30 Ω. Line input test amplitude 2.2 Vpp, f=1 kHz.

DAC Characteristics					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
DAC Resolution			24		bits
Dynamic range (DAC unmuted, A-weighted, min gain)	IDR		100		dB
S/N ratio (full scale signal, no load)	SNR		92		dB
S/N ratio (full scale signal, 30 ohm load)	SNRL		90		dB
Total harmonic distortion, -3dB level, no load	THD		0.01		%
Total harmonic distortion, -3dB level, 30 ohm load	THDL		0.05		%
Crosstalk (L/R to R/L), 30 ohm load, without CBUF [1]	XTALK1		-75		dB
Crosstalk (L/R to R/L), 30 ohm load, with CBUF	XTALK2		-54		dB
Gain mismatch (L/R to R/L)	GERR	-0.5		0.5	dB
Frequency response	AERR	-0.05		0.05	dB
Full scale output voltage	LEVEL		1.0		Vrms
Deviation from linear phase	PH		0	5	°
Analog output load resistance	AOLR		30[2]		Ω
Analog output load capacitance	AOLC			100[3]	pF
DC level, V_{ref}=1.2 V (CBUF, LEFT, RIGHT)	VREF12	1.1	1.2	1.3	V
DC level, V_{ref}=1.6 V (CBUF, LEFT, RIGHT)	VREF16	1.5	1.6	1.7	V
CBUF disconnect current (short-circuit protection)			130	200	mA

[1] Loaded from Left/Right pin to analog ground via 100 µF capacitors.
[2] AOLR may be lower than *Typical*, but distortion performance may be compromised. Also, there is a maximum current that the internal regulators can provide.
[3] CBUF must have external 10 Ω + 47 nF load, LEFT and RIGHT must have external 20 Ω + 10 nF load for optimum stability and ESD tolerance.

3.4 Analog Characteristics of Audio Inputs

ADC Characteristics					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
ADC Resolution			24		bits
Line input amplitude			2200	2800[1]	mVpp AC
Line input Total Harmonic Distortion	LTHD		0.015	0.10	%
Line input S/N Ratio	LSNR	80[2]	90	100	dB
Sample rate		24		192	kHz
Line input impedance			100		kΩ

[1] Above typical amplitude the Harmonic Distortion increases.
[2] Limit Min due to noise level of production tester.

3.5 Digital Characteristics

TBD

3.6 Power Consumption

TBD

3.6.1 Digital Power Consumption

TBD

3.6.2 Analog Power Consumption

TBD

3.6.3 I/O Power Consumption

TBD

3.6.4 Example Power Consumption

TBD

4 Package and Pin Descriptions

4.1 QFN-88 Package

QFN-88 is a 10x10x0.75 mm, lead (Pb) free and RoHS-compliant package. RoHS is a short name of *Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment*.

Package and pin dimensions are shown in Figures 4 and 5. For more information about the QFN-88 package and its dimensions visit *http://www.vlsi.fi/en/support/download.html* .

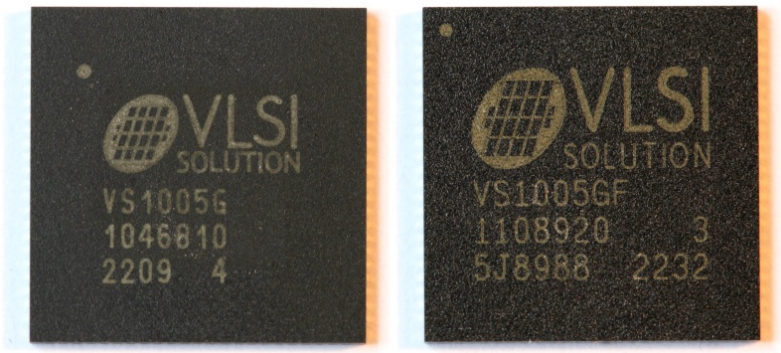


Figure 1: VS1005g QFN-88 (VS1005G and VS1005G-F product variants) top view photo, two different marking styles. This is a similar package to VSRVES01.

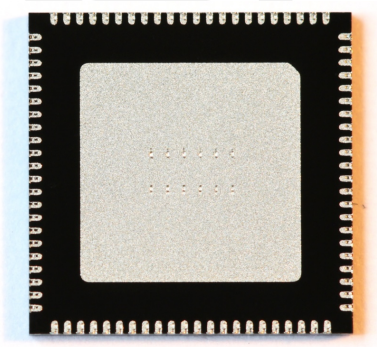


Figure 2: VSRVES01 QFN-88 bottom view photo, pin 1 top right

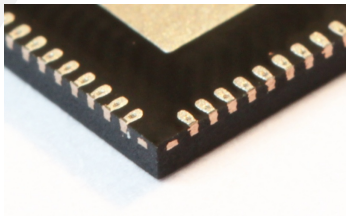


Figure 3: VSRVES01 QFN-88 bottom corner view photo

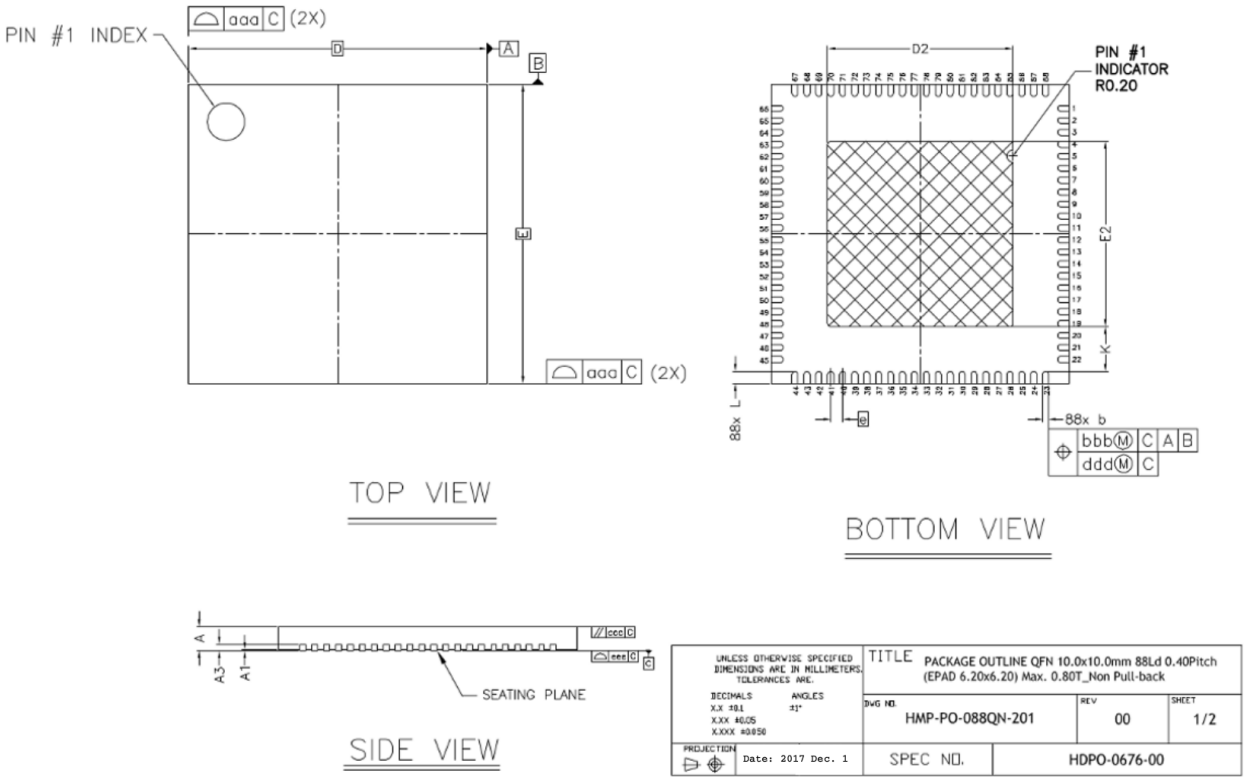


Figure 4: VSRVES01 QFN-88 mechanical drawing, page 1/2

COMMON DIMENSIONS			
SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.15	0.20	0.25
D		10.00 BSC	
E		10.00 BSC	
D2	6.10	6.20	6.30
E2	6.10	6.20	6.30
e		0.40 BSC	
L	0.35	0.40	0.45
K	0.20		
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	

NOTES :

1. DRAWING CONFORM TO JEDEC REFERENCE MO-220.
2. DIMENSIONING AND TOLERANCING SCHEMES CONFORM TO ASEM Y14.5M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. HATCH AREA IS SOLDERABLE EXPOSED PAD.

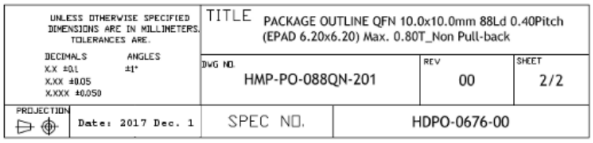


Figure 5: VSRVES01 QFN-88 mechanical drawing, page 2/2

4.2 VSRVES01 Pin Descriptions

Full pin list details TBD.

Pin Name	QFN Pin	Pin Type	GPIO Port:Bit	Primary Function
GPLATE	(0)	GND		Center analog and digital ground plate, use multiple vias to create low-impedance connection to ground plane on PCB! See also pin VREF_0V!

Left Pin Name	QFN Pin	Pin Type	GPIO Port:Bit	Primary Function
DDR_CA5	1			
DDR_CA6	2			
DDR_CA9	3			
DDR_CA8	4			
DDR_CA7	5			
CVDD0	6	CPWR		Core power supply
DDR_DQ15	7			
DDR_DQ14	8			
LVDD0	9			
DDR_DQ13	10			
DDR_DQ12	11			
DDR_DQ11	12			
DDR_DQ10	13			
DDR_DQ9	14			
DDR_DQ8	15			
DDR_DQST1	16			
DDR_DQSC1	17			
DDR_DM1	18			
LVDD1	19			
DDR_DM0	20			
DDR_DQSC0	21			
DDR_DQST0	22			

Bottom Pin Name	QFN Pin	Pin Type	GPIO Port:Bit	Primary Function
DDR_DQ7	23			
DDR_DQ6	24			
DDR_DQ5	25			
DDR_DQ4	26			
LVDD2	27			
DDR_DQ3	28			
CVDD1	29	CPWR		Core power supply
DDR_DQ2	30			
DDR_DQ1	31			
DDR_DQ0	32			
DDR_CKE	33			
DDR_CA2	34			
DDR_CA1	35			
LVDD3	36			
DDR_CA0	37			
DDR_CA3	38			
DDR_CA4	39			
DDR_CSX	40			
DDR_CK	41			
DDR_CK	42			
RV_RX	43	DI***		RV: UARTBOOT RX
RV_TX	44	DO		RV: UARTBOOT TX

Right Pin Name	QFN Pin	Pin Type	GPIO Port:Bit	Primary Function
TXC	45			
TXD0	46			
TXD1	47			
TXD2	48			
TXD3	49			
TX_CTL	50			
RXC	51			
RXD0	52			
RXD1	53			
RXD2	54			
RXD3	55			
IOVDD0	56	IOPWR		I/O power supply
RX_CTL	57			
MDIO	58		0:13	MEMS Digital In
MDC	59		0:12	MEMS Clock
CVDD2	60	CPWR		Core power supply
GP0	61			
GP1	62			
SPI_XS	63	DIO***	0:0	VS: SPI Chip Select
SPI_MISO	64	DIO***	0:2	VS: SPI Master In / Slave Out
SPI_CLK	65	DIO***	0:1	VS: SPI Clock
SPI_MOSI	66	DIO***	0:3	VS: SPI Master Out / Slave In

Top Pin Name	QFN Pin	Pin Type	GPIO Port:Bit	Primary Function
TX	67		0:5	VS:UART0 TX
RX	68		0:4	VS:UART0 RX
SD_CLK	69	DIO***	0:6	VS:SD card clock
SD_CMD	70	DIO***	0:7	VS:SD card command line
SD_DAT0	71	DIO***	0:8	VS:SD card data line 0
SD_DAT2	72	DIO***	0:10	VS:SD card data line 2
SD_DAT1	73	DIO***	0:9	VS:SD card data line 1
SD_DAT3	74	DIO***	0:11	VS:SD card data line 3
IOVDD1	75	IOPWR		I/O power supply
XRESET	76	DI		Active low asynchronous reset, schmitt-trigger input
XTALI	77	AI		Crystal input
XTALO	78	AO		Crystal output
TEST	79	DI		Test mode input (active high), connect to ground
LINEINR	80	AI		Line 0 input right
LINEINL	81	AI		Line 0 input left
RCAP	82	AIO		Filtering capacitance for reference
AVDD2	83	APWR		Analog power supply
RIGHT	84	AO		Right channel output
LEFT	85	AO		Left channel output
AVDDMN	86			
DP	87			
DN	88			

Pin type descriptions:

Type	Description
DI	Digital input, CMOS input pad
DIPD	Digital input with weak pull-down resistor (approx. 1 MΩ)
DO	Digital output, CMOS output pad
DIO	Digital input/output
DIOPD	Digital input/output with weak pull-down resistor in input (approx. 1 MΩ)

Type	Description
AI	Analog input
AO	Analog output
AIO	Analog input/output
GND	Ground
PWR	Main power supply
APWR	Analog power supply pin
CPWR	Core power supply pin
IOPWR	I/O power supply pin

Package bottom plate is a ground net and it is connected to ground network in PCB.

NOTE: Unused inputs should not be left floating. Tie either HIGH or LOW as appropriate. At power-up all GPIO is three stated and current leakage from IOVDD is cut. Outputs that are three-statable should only be pulled high or low to ensure signals at power-up and in standby.

Alternate pin functions in VSRVES01 package			
Pin Name	**QFN Pin**	**Pin Type**	**Function**
Analog Line input 1	71	AI	Alternate analog input pin for Line input 1
Analog Line input 2	70	AI	Alternate analog input pin for Line input 2
Analog Line input 1	68	AI	Alternate analog input pin for Line input 1
Analog Line input 2	67	AI	Alternate analog input pin for Line input 2
Digital DA/AD Clock	52	DO	Digital DA/AD clock output, XTALI/2/4
Digital DAC Right	32	DO	DAC right channel digital output, XTALI/2
Digital DAC Left	33	DO	DAC left channel digital output, XTALI/2
DIA1	53	DIPD	Digital ADC 1 input, XTALI/2
DIA2	55	DIPD	Digital ADC 2 input, XTALI/2
DIA3	51	DIPD	Digital ADC 3 input, XTALI/2
TMS	31	DIPD	Jtag Test Mode Select
TDI	32	DIPD	Jtag Test Data In
TDO	33	DO	Jtag Test Data Out
TCK	34	DIPD	Jtag Test Clock
DBGREQ	35	DO	Hardware debug state pin

4.2.1 PCB Layout Recommendations

The following recommendations should be followed to ensure reliable operation.

- Analog power nets that are connected to regulator APWR/CPWR output should have bypass capacitors.

5 Example Schematic

TBD

5.1 Important Tips and Guidelines for Designing VSRVES01 Products

TBD

6 VSRVES01 General Description

TBD

7 Oscillator and Reset Configuration

TBD

8 VSDSP Firmware Operation

TBD

8.1 VSDSP SPI Boot

TBD

8.2 VSDSP UART Boot/Monitor

When byte 0xef is sent to RX at 115200 bps, the firmware enters monitor mode and communicates with **vs3emu**. Memory contents can be displayed, executables can be loaded and run, or the firmware code can be restarted or continued.

The UART is also one convenient way to program the SPI EEPROM, or to send to VSDSP a pieve of software that can quickly read and program an SPI EEPROM image from an SD Card.

9 Document Version Changes

This chapter describes the most important changes to this document.

Version 0.01, 2025-05-07

- First released, *very preliminary* version.

10 Contact Information

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