VS23S040D - 4 Megabit SPI SRAM
with Serial and Parallel Interfaces and Integrated Video Display Controller

Features

- Flexible 1.5V - 3.6V operating voltage
- 524,288 x 8-bit SRAM organization
- Serial Peripheral Interface (SPI) mode 0 compatible
  - Byte, Page and Sequential modes
  - Supports Single, Dual and Quad I/O read and write
  - Fast operation: the whole memory can be filled in 1,048,590 or read in 1,048,591 cycles (Quad-I/O SPI, Quad address mode)
  - XHOLD and XWP pins
- 8-bit Parallel Interface (Simplified 8080 and NAND FLASH Type Interface)
  - Sequential read and write in 4 byte blocks
  - Fast operation, the whole memory can be filled or read in 524,293 cycles
- Integrated Video Display Controller with Video DAC
  - Supports Component and Composite video formats (NTSC, PAL, RGB etc.)
  - Fully configurable by user
  - 9-bit Video DAC and 8x Video PLL
- High operating frequencies
  - Up to 38 MHz for SPI
  - Up to 40 MHz for 8-bit parallel interface
  - Over 35 MHz for Video Display Controller
  - (TBD) MHz for SRAM writes when Video Display Controller enabled
- Active Low-power
  - Read current 1.6 mA at 1 MHz (Single I/O, SO=0, T_A=+85°C, VDD=3.3V)
- Industrial temperature range
  - -40°C to + 85°C
- Pb-Free and RoHS compliant

Description

The VLSI Solution VS23S040D is an easy-to-use and versatile serial SRAM device. The memory is accessed via an SPI compatible serial bus. The device also contains Video Display Controller, which can be configured to continuously output analog composite video from the memory array data to implement a video frame buffer.

Alternatively, a 8-bit parallel interface can be used to access the SRAM instead of the SPI.

To sum up, there are four separate operating modes in VS23S040D:

- SPI Single, Dual, or Quad operation and 4 General Purpose I/O pins
- SPI Single, Dual, or Quad operation and simultaneous Video Display Controller
- 8-bit Parallel Interface operation
- 8-bit Parallel Interface operation and simultaneous Video Display Controller

Applications

- Micro-controller RAM extension
- VoIP and internet data stream buffer
- Audio data buffer
- Video frame buffer

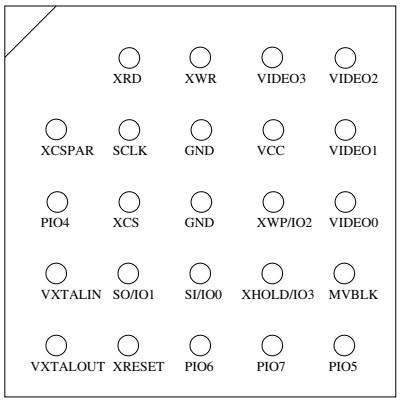


Figure 1: pin out (top view, not to scale)

Operating Modes

3

VS23S040D operates in one of four modes: SPI, SPI and Video Display Controller, 8-bit parallel mode or 8-bit parallel mode and Video Display Controller.

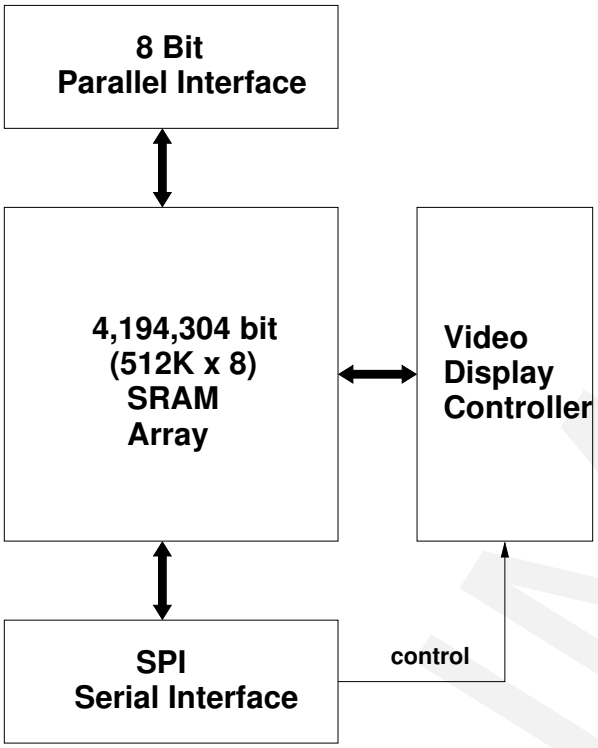


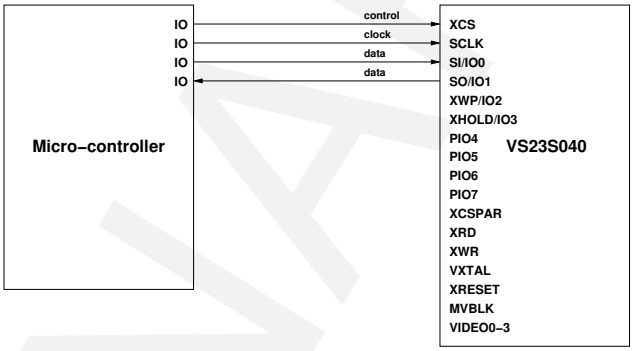
Figure 2: SPI or 8-bit parallel interface and Video Display Controller can be enabled at the same time.

In SPI mode SRAM and control registers can be accessed. Dual-I/O and Quad-I/O modes are used only for SRAM read and write.

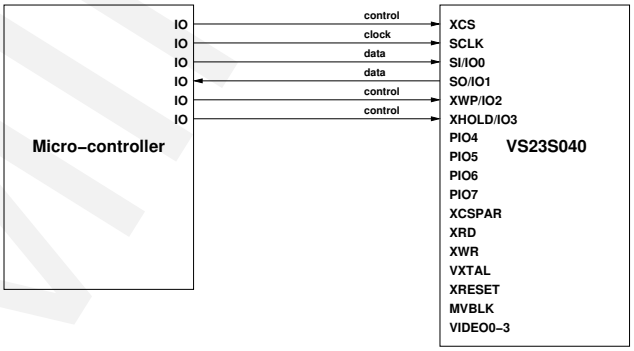
When Video Display Controller is enabled SPI can be used simultaneously. There is an additional limit to maximum SPI access rate in this mode.

When 8-bit parallel interface is used to access SRAM, SPI must be inactive. Video Display Controller can be operational simultaneously. Video Display Controller is controlled only by SPI. There is a limit to maximum access rate for 8-bit parallel interface when Video Display Controller is enabled.

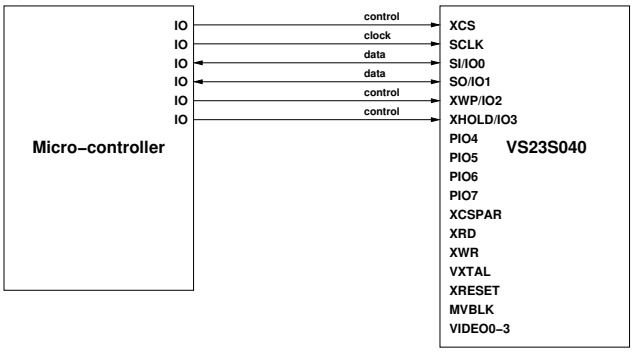
Following are connection examples for different operating modes. Some I/Os are unconnected, because they have internal pull-up or pull-down resistors. Power and ground connections are not shown.



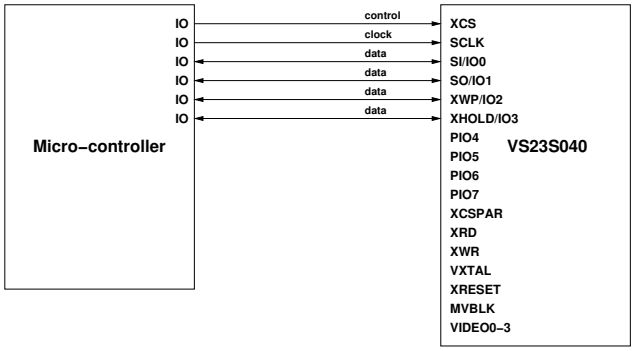
SPI connection, minimum configuration



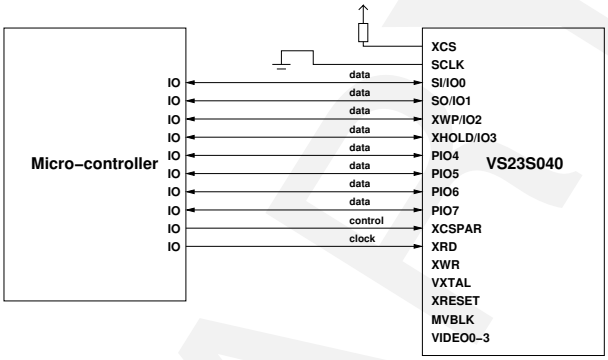
SPI connection, basic configuration



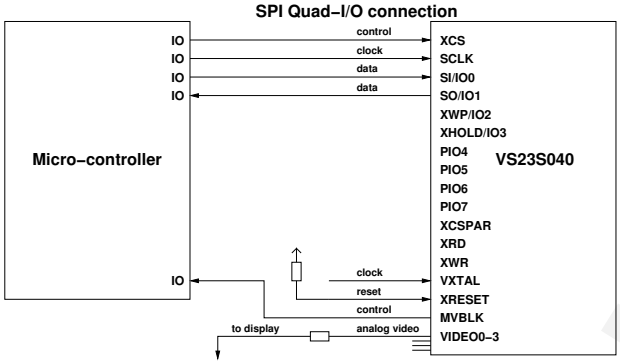
SPI Dual–I/O connection



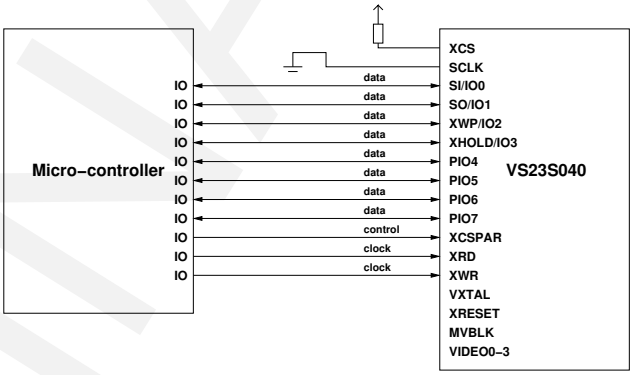
SPI Quad−I/O connection



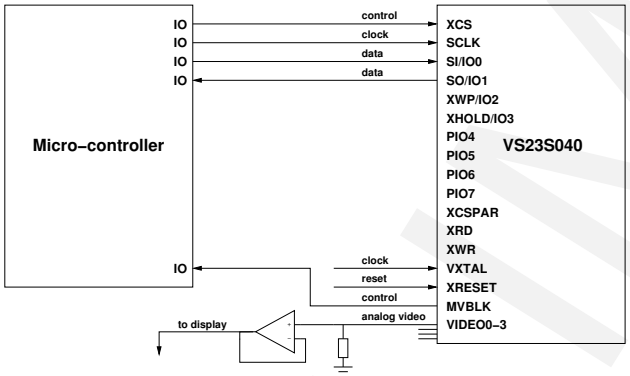
8−bit parallel interface (minimum configuration, one clock is enough)



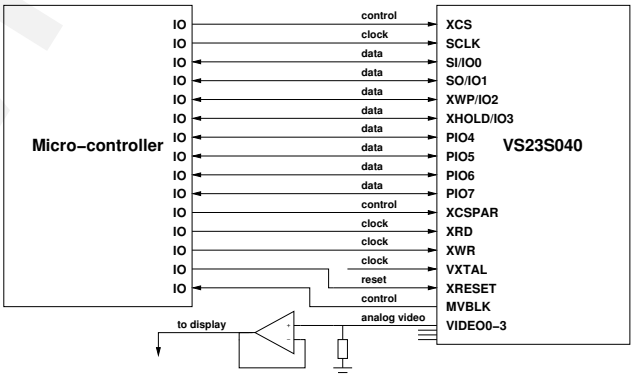
SPI connection (minimum configuration), video generator enabled



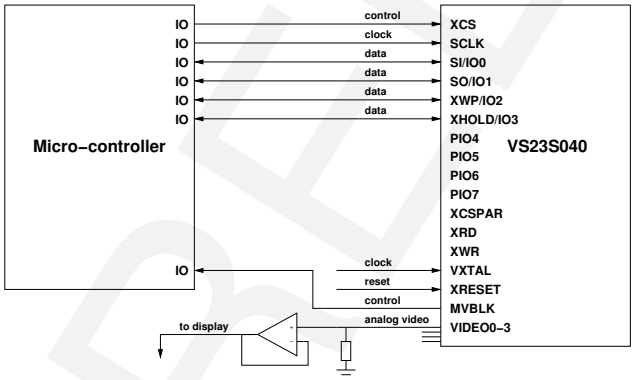
8−bit parallel interface



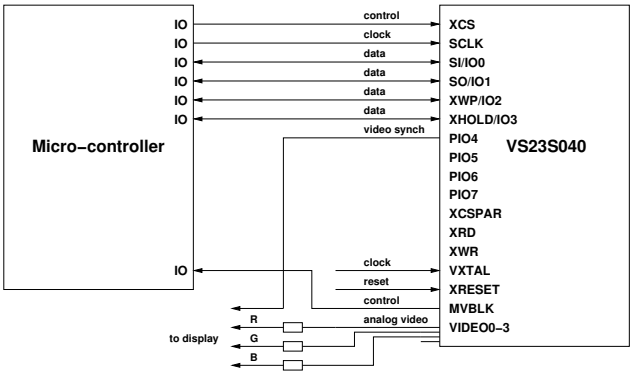
SPI connection (minimum configuration), video generator enabled and video buffer



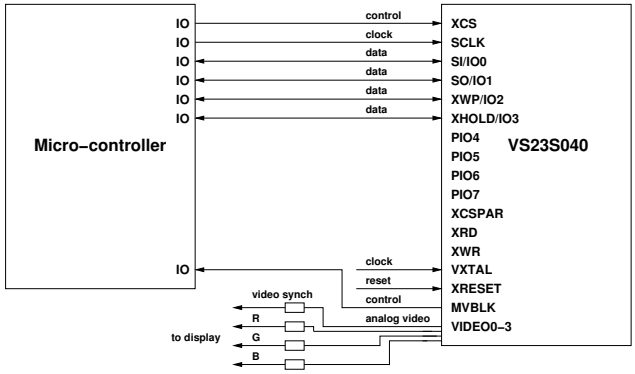
8−bit parallel interface, video generator enabled, video buffer (SPI for video generator control when 8−bit interface is not active)



SPI Quad−I/O connection, video generator enabled, video buffer



SPI Quad−I/O connection, video generator enabled, VGA mode



SPI Quad−I/O connection, video generator enabled, VGA mode (analog video synch generation)

Contents

List of Figures

1 Disclaimer

This is a *preliminary* data sheet. All properties and figures are subject to change.

2 Definitions

B Byte, 8 bits

b Bit

CSClk Clock, which frequency is Color Subcarrier Frequency of a video format.

GPIO General Purpose I/O

LSB Least Significant Bit

MSB Most Significant Bit

NTSC National Television System Committee video format, color subcarrier frequency is 3.579545 MHz.

PAL Phase Alternating Line video format, color subcarrier frequency is 4.43361875 MHz.

POR Power On Reset

SPI Serial Peripheral Interface

SRAM Static Random Access Memory

TBD To Be Defined

U, V Chrominance components (color information)of video signal

VClk Video Display Controller clock of the VS23S040D. It can come directly from VXTAL oscillator or can be generated on-chip by 8x PLL from VXTAL pins. **VClk frequency has to be 8 times the color subcarrier frequency of the selected analog video format.**

$$F_{VClk} = 8 \times F_{CSClk}$$

If on-chip PLL is used, the VXTAL clock frequency is 3.579545 MHz for NTSC and 4.43361875 MHz for PAL video. If Video Display Controller clock is directly from the VXTAL pins without using the on-chip PLL, then VXTAL clock frequency is 28.63636 MHz for PAL and 35.46895 for NTSC video.

Y Luna component (the brightness) of video signal

3 Electrical Characteristics & Specifications

3.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Positive Supply	VDD	-0.3	3.6	V
Current at any non-power pin[1]			±50	mA
Voltage at any digital input		-0.3	VDD+0.3[2]	V
Operating temperature		-40	+85	°C
Storage temperature		-65	+150	°C
ESD protection on any pin[3]		2.0		kV

[1] Higher current can cause latch-up.
[2] Must not exceed 3.6 V
[3] Human Body Model (HBM) MIL-STD-883E Method 3015.7

3.2 DC Characteristics

T_A = -40 ... +85 °C

Parameter	Min	Max	Unit	Test Conditions
Positive supply voltage	1.5	3.6	V	
High-level input voltage	$0.7\times$VDD	VDD+0.3[1]	V	
Low-level input voltage	-0.2	$0.3\times$VDD	V	
Low-level input voltage	-0.2	$0.25\times$VDD	V	Any Schmitt-trigger pin
High-level output voltage	$0.7\times$VDD		V	I_O = -1.0 mA
Low-level output voltage		$0.3\times$VDD	V	I_O = 1.0 mA
I/O leakage current [2]	-8.00	8.00	μA	Pin as input or High-Z
Pull-up current	-30.0	-4.00	μA	Any pull-up pin
Pull-down current	2.00	20.0	μA	Any pull-down pin
I/O capacitance [3]		25	pF	VDD=0V, f=0.5 MHz, T_A=+25 °C
RAM data retention voltage [3,4]		0.9	V	
Start-up time after power-up [3]		100	μs	
DAC output load	75		Ω	
DAC output level (code 000h) (code 1FEh)	-15 1.245	15 1.400	mV V	VDD $\geq$ 3.0 V, 75 Ω load

[1] Must not exceed 3.6V
[2] Excluding the pins with pull-up or pull-down resistors
[3] This parameter is periodically sampled and is not 100% tested.
[4] This is the limit to which VDD can be lowered without losing RAM data.

3.3 AC Characteristics

3.3.1 General

VDD = 3.3 V, T_A = -40 ... +85 °C

Parameter	Symbol	Min	Max	Unit
Data clock high time	Tclkh	$0.5 * T_{MIN}$ [1]		ns
Data clock low time	Tclkl	$0.5 * T_{MIN}$ [1]		ns
Data clock rise time [2]	Tclkr		2	μs
Data clock fall time [2]	Tclkf		2	μs
Data in setup time	Tds	3		ns
Data in hold time	Tdh	8		ns
Output disable time [2]	Tdis		18	ns
Output valid time	Tv		34	ns
Output hold time	Toh	8		ns

[1] T_{MIN} is the minimum clock cycle time in each mode. For SPI mode it is 1/max(F_{SCLK}) and for 8-bit Parallel Mode it is 1/max(F_{XRD_XWR}).
[2] This parameter is periodically sampled and is not 100% tested.

3.3.2 SPI Mode

VDD = 3.3 V, T_A = -40 ... +85 °C

Parameter	Symbol	Min	Max	Unit	Test Conditions
SPI clock frequency [1]	F_{SCLK}		26 31	MHz MHz	VDD = 1.5 V VDD $\geq$ 1.8 V
XCS high time	Txcshi	38 32		ns ns	VDD = 1.5 V VDD $\geq$ 1.8 V
XCS setup time	Txcss	5		ns	
XCS hold time	Txcsh	0		ns	
XHOLD setup time	Txhs	3		ns	
XHOLD hold time	Txhh	2		ns	
XHOLD low to output High-Z [2]	Txhlz	5		ns	
XHOLD high to output valid [2]	Txhhz		18	ns	
XWP setup time	Txws	2		ns	
XWP hold time	Txwh	2		ns	

[1] When used with an external micro-controller the maximum SPI frequency is based on the total of VS23S040D and micro-controller I/O-delays and routing delays of the card.
[2] This parameter is periodically sampled and is not 100% tested.

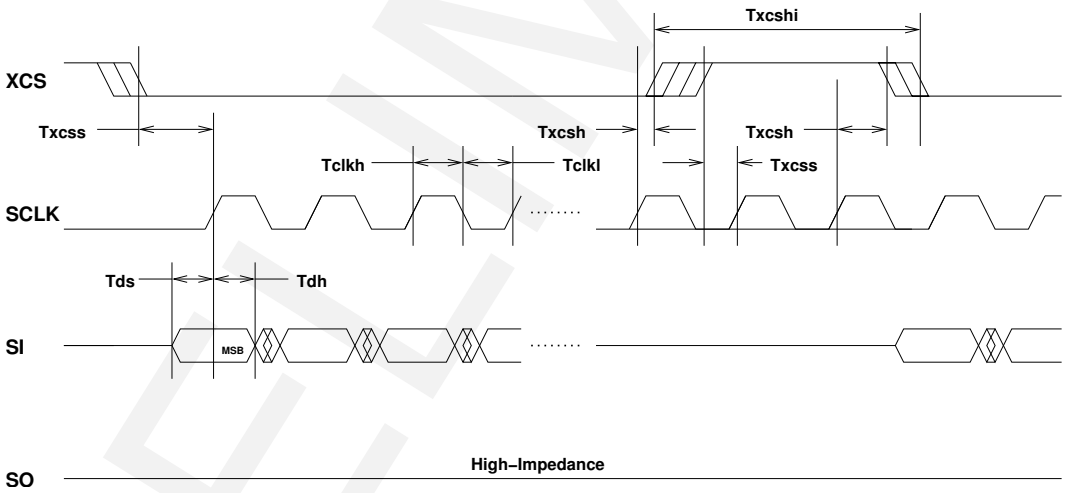


Figure 3: SPI Input Timing

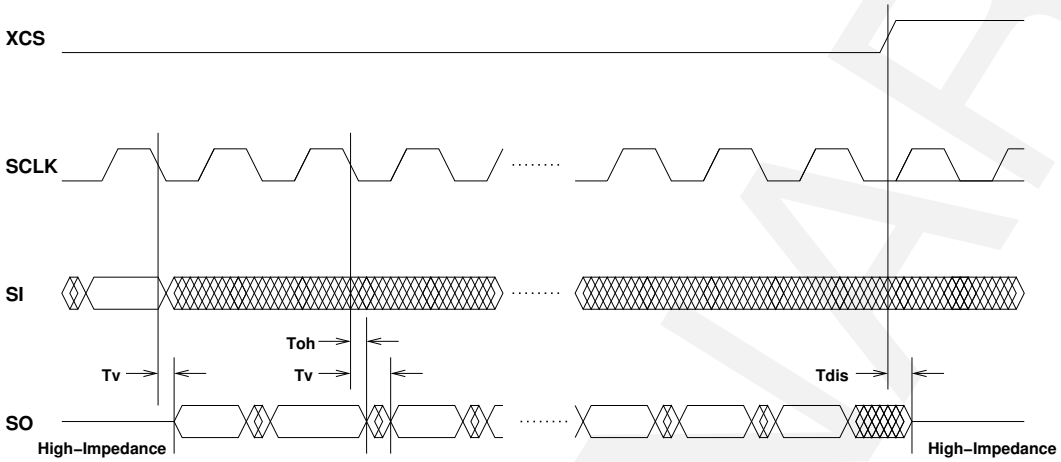


Figure 4: SPI Output Timing

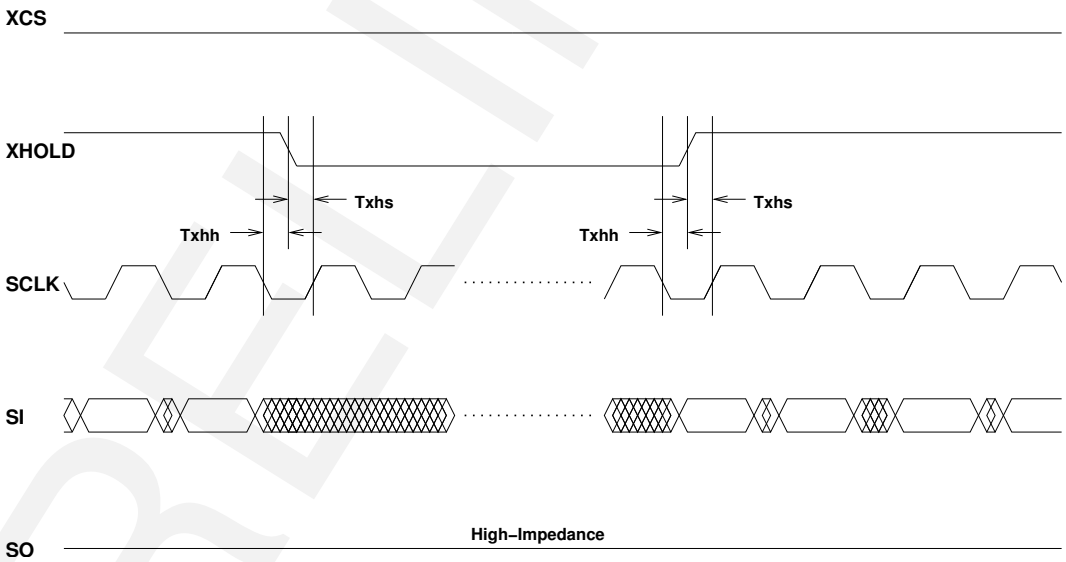


Figure 5: XHOLD Timing, SPI and Dual-I/O Input Modes. Notice that internal address counter does not increment, when XHOLD is low.

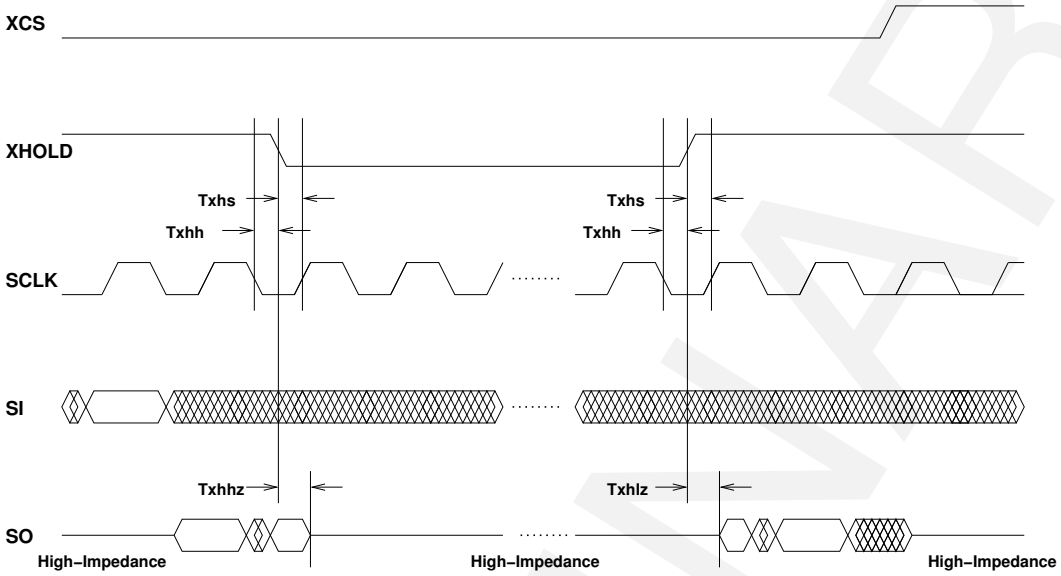


Figure 6: XHOLD Timing, SPI and Dual-I/O Output Modes. Notice that internal address counter does not increment, when XHOLD is low.

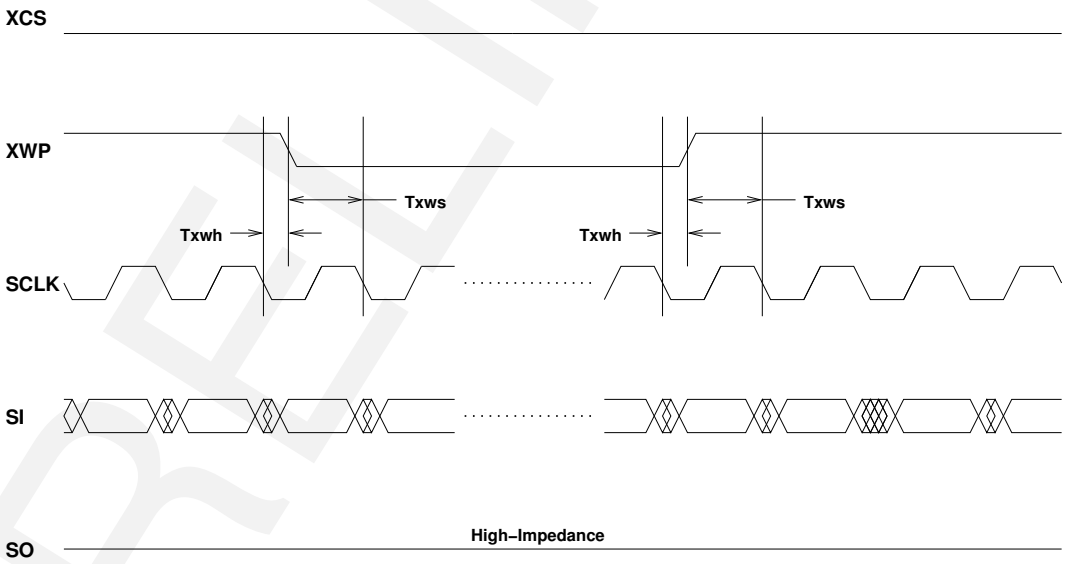


Figure 7: XWP Timing, SPI and Dual-I/O Modes. Notice that internal address counter increments, when XWP is low.

3.3.3 Video Display Controller Mode

VDD $\geq$ 3.0 V, T_A = -40 ... +85 °C

Parameter	Symbol	Min	Typ [3]	Max	Unit	Test Conditions
VXTAL frequency when PLL used	F_{VXTALP}	2.6 [1]		4.5	MHz	
VXTAL frequency when PLL not used	$F_{VXTALXP}$	-		35.5	MHz	
XRESET active time [1,2]	Txresl	T_{VXTAL} +20			ns	
XRESET inactive to ready [1]	Txresv			$4 * T_{VClk}$ +10	ns	
High current mode, 75 Ω load						
Output level:						
code 000h (Sync level) code 0FFh	Levprhc	-18 555	-2 667	18 690	mV mV	Protoline
code 066h (Black level) code 165h (White level)	Levpihc	217 795	264 937	285 1073	mV mV	Picture line
code 1FEh	Levdmhc	1.200	1.356	1.400	V	Direct mode
Output rise time	Tdacorfhc				ns	
Output settling time	Tdacoshc				ns	
Differential nonlinearity error	DNLdachc		+1.4/-1.4 +1.2/-1.0	+2.3/-2.3 +2.3/-2.3	LSB LSB	Protoline Picture line
Integral nonlinearity error	INLdachc		+1.4/-1.7 +1.6/-1.3	+2.3/-3.3 +2.7/-2.7	LSB LSB	Protoline Picture line
Low current mode, 75 Ω load						
Output level:						
code 000h (Sync level) code 0FFh	Levprlc	-3 45	-1.7 53	3 57	mV mV	Protoline
code 066h (Black level) code 165h (White level)	Levpilc	17 64	20 76	24 80	mV mV	Picture line
Output rise time	Tdacorflc				ns	
Output settling time	Tdacoslc				ns	

[1] This parameter is periodically sampled and is not 100% tested.
[2] Note that XRESET affects only to Video Display Controller logic. Video Display Controller control registers are not reset by XRESET.
[3] Typical values are given at +25 °C.

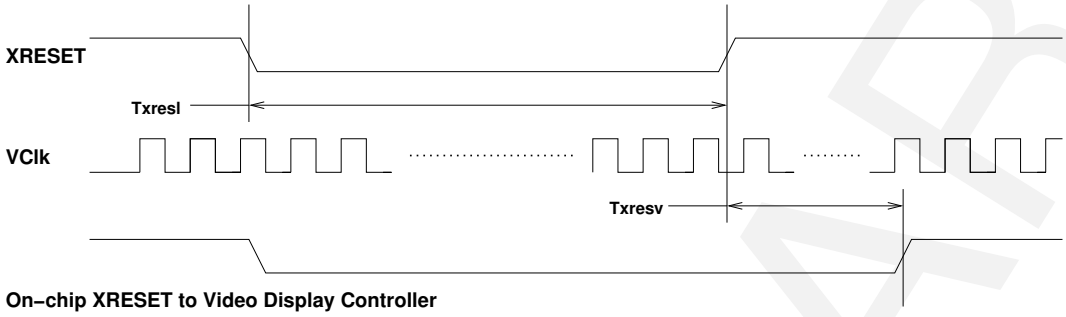


Figure 8: XRESET Timing

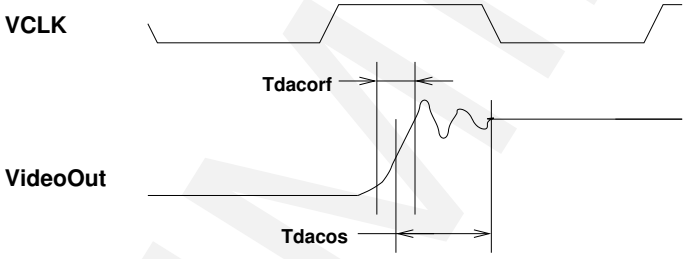


Figure 9: VideoOut Timing

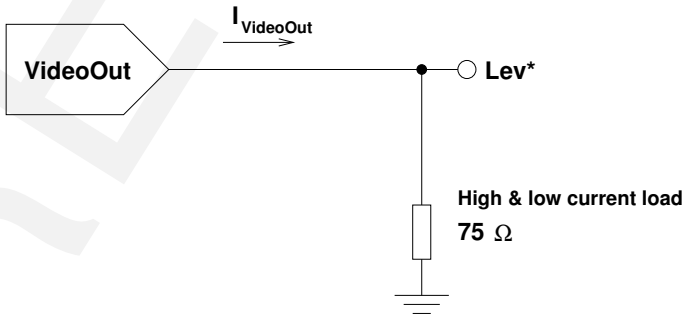


Figure 10: VideoOut Level Measurement

3.3.4 8-bit Parallel Interface Mode

VDD = 3.3 V, T_A = -40 ... +85 °C

Parameter	Symbol	Min	Max	Unit	Test Conditions
Clock frequency [1]	F_{XRD_XWR}		26	MHz	VDD = 1.5 V
			28	MHz	VDD = 1.8 V
			33	MHz	VDD = 3.0 V
XCSPAR high time	Txcphi	38		ns	VDD = 1.5 V
		36		ns	VDD = 1.8 V
		30		ns	VDD = 3.0 V
XCSPAR setup time	Txcps	2		ns	
XCSPAR hold time	Txcph	0		ns	

[1] When used with an external micro-controller the maximum 8-bit Parallel Interface frequency is based on the total of VS23S040D and micro-controller I/O-delays and routing delays of the card.

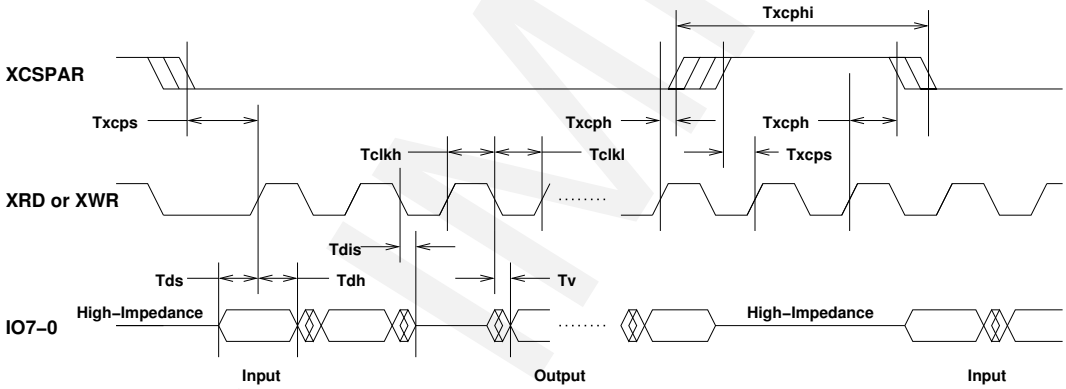


Figure 11: 8-bit Parallel Interface Timing

AC Test Conditions

AC Waveform:	
Input pulse level	$0.1\times$VDD to $0.9\times$VDD
Input rise/fall time	(TBD) ns
Operating temperature	-40 °C to +85 °C
C_L = (TBD) pF	
Timing Measurement Reference Level:	
Input	$0.5\times$VDD
Output	$0.5\times$VDD

3.4 Current Consumption

VDD = 3.3 V, T_A = +25 °C, XCS=VDD, SI=SO=SCLK=GND, other inputs connected to VDD or GND by on-chip pull-up or pull-down resistors of the pins.

Parameter	Min	Typ	Max	Unit	Test Conditions
Stand-by current		160 - 360	(TBD) 1.4 [1] 4.8 [1]	µA mA mA	 T_A = +85 °C T_A = +125 °C

[1] This parameter is periodically sampled and is not 100% tested.

3.4.1 SPI Mode

VDD = 3.3 V, T_A = +85 °C, these parameters are periodically sampled and are not 100% tested.

Parameter	Min	Typ	Max	Unit	Test Conditions
VDD current, SPI single output read			1.6 2.0 3.7	mA mA mA	F_{SCLK} = 1 MHz, SO = 0 F_{SCLK} = 10 MHz, SO = 0 F_{SCLK} = 24 MHz, SO = 0
VDD current, SPI single port write & read, two patterns[1]		0.3 - 0.7 1.3 - 2.9		mA mA	F_{SCLK} = 1 MHz, T_A = +25 °C F_{SCLK} = 10 MHz, T_A = +25 °C

[1] Current is very much data-dependent.

3.4.2 Video Display Controller Mode

VDD = 3.3 V, T_A = +25 °C, these parameters are periodically sampled and are not 100% tested.

Parameter	Min	Typ	Max	Unit	Test Conditions
VDD current, Video Display Controller on		15 - 75		mA	75 Ω load

3.4.3 8-bit Parallel Interface Mode

VDD = 3.3 V, T_A = +85 °C, these parameters are periodically sampled and are not 100% tested.

Parameter	Min	Typ	Max	Unit	Test Conditions
VDD current, parallel read			1.8	mA	F_{XRD_XWR} = 1 MHz, data out = 00h
			2.6	mA	F_{XRD_XWR} = 10 MHz, data out = 00h
			4.6	mA	F_{XRD_XWR} = 24 MHz, data out = 00h
VDD current, parallel read & write, increasing data[1]		0.4 - 1.1		mA	F_{XRD_XWR} = 1 MHz, T_A = +25 °C
		1.7 - 6.6		mA	F_{XRD_XWR} = 10MHz, T_A = +25 °C
		2.4 - 7.7		mA	F_{XRD_XWR} = 15MHz, T_A = +25 °C

[1] Current is very much data-dependent.

4 Packages and Pin Descriptions

4.1 BGA24

5 mm x 5 mm BGA24 is a lead (Pb) free and also RoHS compliant package. RoHS is a short name of *Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment*.

BGA24 package dimensions can be found at *http://www.vlsi.fi/fileadmin/quality/bga24_5x5mm_outline.pdf*.

The VS23S040D has the following pin out:

Pin Name	BGA24 Pin	Pin Type	Function	Initial State
XRD	A2	DISPU	Clock of 8-bit parallel interface	IH
XWR	A3	DISPU	Clock of 8-bit parallel interface	IH
VIDEO3	A4	AO	Current-mode analog composite video output #3	I
VIDEO2	A5	AO	Current-mode analog composite video output #2	I
XCSPAR	B1	DISPU	Active low chip select of 8-bit parallel interface	IH
SCLK	B2	DIS	SCLK for SPI	I
GND	B3	GND	Ground	
VCC	B4	PWR	Power supply	
VIDEO1	B5	AO	Current-mode analog composite video output #1	I
PIO4	C1	DIOPD	IO4 for 8-bit parallel interface / GPIO0 / VGP0 for Video Display Controller	IL
XCS	C2	DIS	Active low chip select for SPI	I
GND	C3	GND	Ground	
XWP/IO2	C4	DIOSPU	Active low write protect for SPI and Dual-I/O SPI / IO2 for Quad-I/O SPI and 8-bit parallel interface	IH
VIDEO0	C5	AO	Current-mode analog composite video output #0	I
VXTALIN	D1	DIC	Clock for Video Display Controller	I
SO/IO1	D2	DIO	SO for SPI / IO1 for Dual-I/O and Quad-I/O SPI and 8-bit parallel interface	I
SI/IO0	D3	DIO	SI for SPI / IO0 for Dual-I/O and Quad-I/O SPI and 8-bit parallel interface	I
XHOLD/IO3	D4	DIOSPU	Active low Hold for SPI and Dual-I/O SPI / IO3 for Quad-I/O SPI and 8-bit parallel interface	IH
MVBLK	D5	DO	Video Display Controller #0 block move active	OL
VXTALOUT	E1	DOC	Clock for Video Display Controller	I
XRESET	E2	DISPD	Active low reset for Video Display Controller	IL
PIO6	E3	DIOPD	IO6 for 8-bit parallel interface / GPIO2 / VGP2 for Video Display Controller	IL
PIO7	E4	DIOPD	IO7 for 8-bit parallel interface / GPIO3 / VGP3 for Video Display Controller	IL
PIO5	E5	DIOPD	IO5 for 8-bit parallel interface / GPIO1 / VGP1 for Video Display Controller	IL

Pin types:

Type	Description
AO	Current-mode analog output, external series resistor needed for voltage
DIO	Digital input/output
DIOPD	Digital input/output with Pull-Down resistor
DIOSPU	Digital input/output with Pull-Up resistor, Schmitt-trigger
DIS	Digital input, Schmitt-trigger
DISPD	Digital input with Pull-Down resistor, Schmitt-trigger
DISPU	Digital input with Pull-Up resistor, Schmitt-trigger
DIC	Digital input, clock oscillator
DOC	Digital output, clock oscillator
DO	Digital output
GND	Ground pin
PWR	Power supply pin

Initial States of pins after power-up:

Initial State	Description
I	Input, floating (3-state)
IL	Input, on-chip Pull-Down resistor
IH	Input, on-chip Pull-Up resistor
OL	Output, driven low

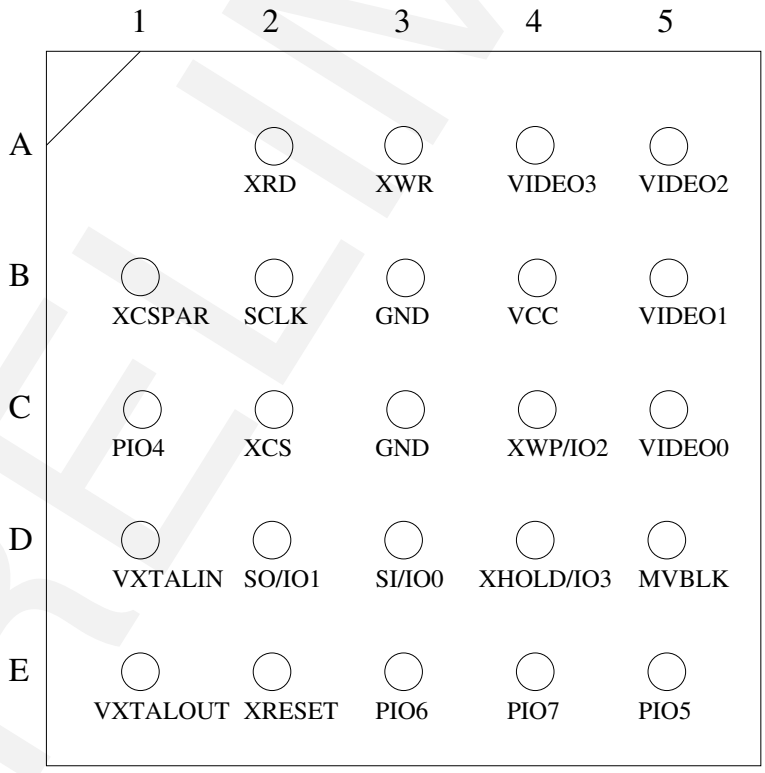


Figure 12: BGA24 pin out (top view, not to scale)

5 Connection Guidelines

To minimize power supply noise connect suitable by-pass capacitors between VCC supply pins and GND. Place by-pass capacitors as near as possible to VS23S040D for best effect.

VXTALIN and VXTALOUT are crystal oscillator pins for Video Display Controller.

Make sure that there is the lowest possible capacitive coupling between different clocks and chip selects (SCLK, XRD, XWR, VXTALIN, VXTALOUT, XCS and XCSPar) and particularly to data signals on the circuit board. This is for minimizing interference between these signals.

Video0-3 are current-mode analog outputs which can be connected to a display via two 22 Ω series resistors and a transient suppressor (for example CG0603MLA-5.5ME) providing some extra protection or by using an op-amp buffer.

6 Device Operation

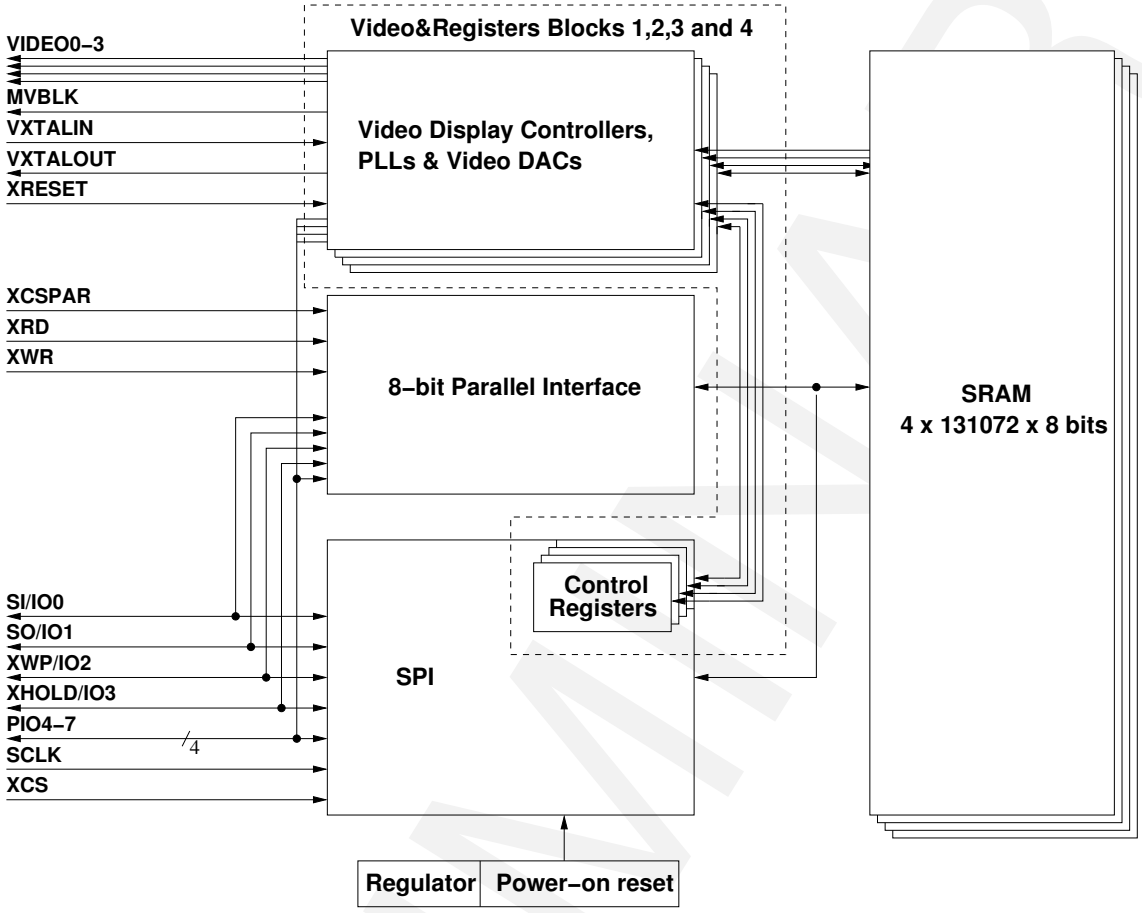


Figure 13: Device organization diagram

The device consists of following main blocks: SPI, Video Display Controllers, 8-bit Parallel Interface and SRAM. SPI and Video Display Controllers can be enabled simultaneously and also 8-bit Parallel Interface and Video Display Controllers can be enabled at the same time. However, SPI and 8-bit Parallel Interface have to be used separately because they share I/O. The SRAM consists of four blocks, which appear to user as a single unit.

There are four Video Display Controller instances. Each of them can access and use a quarter of the total SRAM. The first Video Display Controller uses the memory from 0 to 128 kB (addresses 00000h to 1FFFFh), the 2nd uses from 128 kB to 256 kB (addresses 20000h to 3FFFFh), the 3rd from 256 kB to 384 kB (addresses 40000h to 5FFFFh) and last one uses memory from 384 kB to 512 kB (addresses 60000h to 7FFFFh). Each Video Display Controller has their own control registers which can be accessed separately if needed. Also there are all other control registers for each quarter of the total SRAM, which can also be set separately if such need arises (usually there is no need). The Video Display Controller and control register logic for each quarter of SRAM is called **Video&Registers Block**.

6.1 SPI

The VS23S040D is controlled by a set instructions that are sent from a host controller, commonly referred as SPI Master. The SPI Master communicates with the VS23S040D via the SPI bus which is comprised of five signal groups: Chip Select (XCS), Serial Clock (SCLK), Serial Input (SI, also SO in Dual-I/O mode and XWP and XHOLD in Quad-I/O mode), Serial Output (SO, also SI in Dual-I/O mode and XWP and XHOLD in Quad-I/O mode) and Control (XWP and XHOLD in Single and Dual-I/O modes).

The VS23S040D supports SPI protocol operation mode 0, which is very commonly used. Data is always latched in on the rising edge of the SCLK and always output on the falling edge of the SCLK. SPI mode 0 is used in Single, Dual-I/O and Quad-I/O modes.

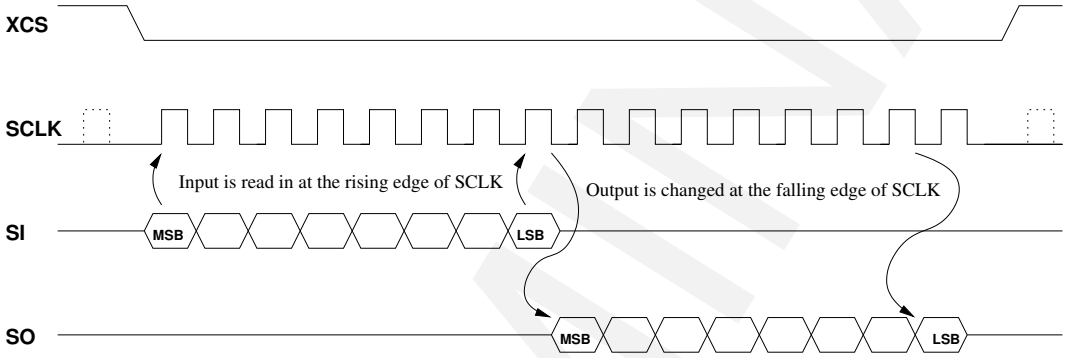


Figure 14: SPI Mode 0

SPI block does not have a separate Reset pin. There is an on-chip power-up delay logic, which is used to reset the selected SPI registers. SPI block logic is clocked by the SCLK pin. Following is a table describing the registers of the VS23S040D.

Register	Symbol	R/W	Default Value	Initialization
General				
Status	STATUS	RW	00h	Power-Up
Manufacturer and Device ID	ID	R	2Bh	Power-Up
GPIO Control	GPIOCTRL	RW	00h	Power-Up
GPIO State	GPIOSTATE	R	0Ch	Pull-down and pull-up resistors
Video&Registers Block Selection	MDACC	RW	00h	Power-Up
Video Display Controller				
Line Start	PGLPXST	W	000h	Power-Up
Line End	PGLPXEND	W	000h	Power-Up
Line Length	PGLPXLEN	W	000h	Power-Up
Index Start	PGIDXST	W	0000h	Power-Up
Control1	PGCTRL1	W	0000h	Power-Up
Control2	PGCTRL2	W	0000h	Power-Up
V Table	PGVTBL	W	0000h	Power-Up
U Table	PGUTBL	W	0000h	Power-Up
Program	PGPRGM	W	0000 0000h	Power-Up
Line Value	PGCURRL	R	0000h	Power-Up
Block Move Control1	PGBMCTRL1	W	0 0000 0000h	Power-Up
Block Move Control2	PGBMCTRL2	W	0000 0000h	Power-Up

6.1.1 Byte, Page and Sequential Operation Modes

Bits 7 to 6 of the Status register select these three SPI Operation Modes. These modes affect SPI Single, Dual and Quad I/O SRAM operations. Before these control bits are adjusted, it is advised to set Video&Registers Block Selection register bits to 00h (default state also) so that all four Video&Registers Block and their corresponding SRAM parts receive then similar setup for these bits.

Byte Operation This mode is selected when Mode bits are “00”. Read and write operations are limited to one byte in this mode i.e. address does not increment after each written or read byte. After command and 24-bit address byte data is read from or written to given SRAM address every time after subsequent 8 (Single), 4 (Dual-I/O) or 2 (Quad-I/O) SCLK cycles.

Page Operation This mode is selected when Mode bits are “10”. VS23S040D has 16384 pages of 32 bytes. In page mode reads and writes are limited to the page selected by the given address. After each written or read byte the SRAM address is increased automatically. When the last address of page is reached the accessing will continue from the first address of the page.

Sequential Operation This mode is selected when Mode bits are “01”. In this mode the entire SRAM array can be accessed in one operation. The address counter is increased automatically

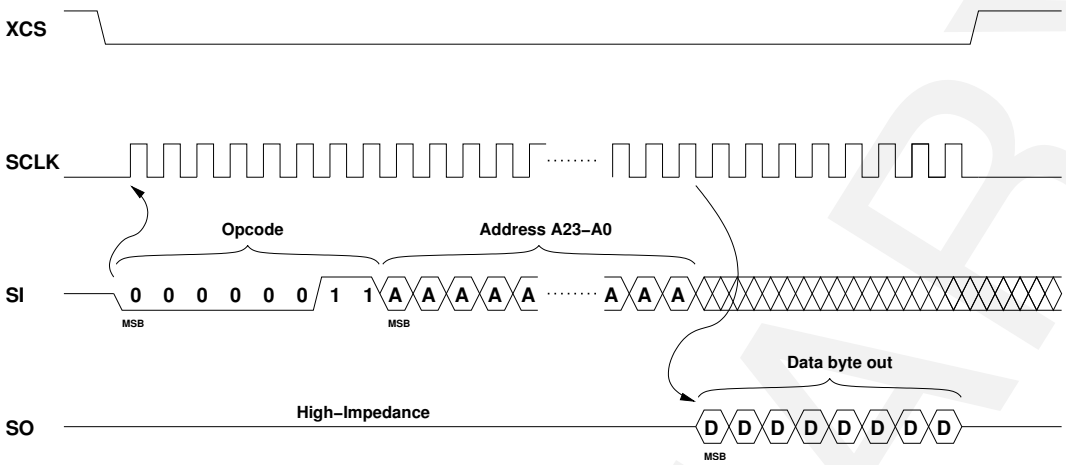


Figure 15: SPI Byte read

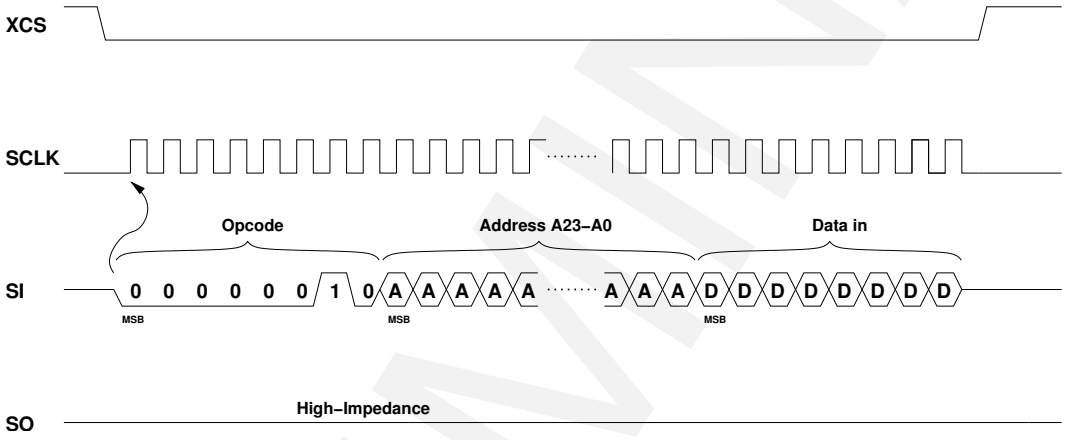


Figure 16: SPI Byte write

and when the last address 7FFFFh of the SRAM is reached the address counter returns to value 00000h.

6.1.2 Dual-I/O and Quad-I/O Operation

In Dual-I/O SPI mode two data bits are read or written during one SCLK cycle. SI/IO0 pin is the lower bit and SO/IO1 pin is the higher bit in Dual-I/O mode. Both pins are inputs during the write and outputs during the read.

In Quad-I/O SPI mode four data bits are read or written during one SCLK cycle. SI/IO0 pin is the lowest bit, SO/IO1 pin is the second bit, XWP/IO2 is the third bit and finally XHOLD/IO3 is the fourth bit in Quad-I/O mode. The pins are inputs during the write and outputs during the read.

In these modes the SPI command is still given in one-bit SPI mode. The address can be given either in one-bit SPI mode or multi-bit SPI mode depending on the given command.

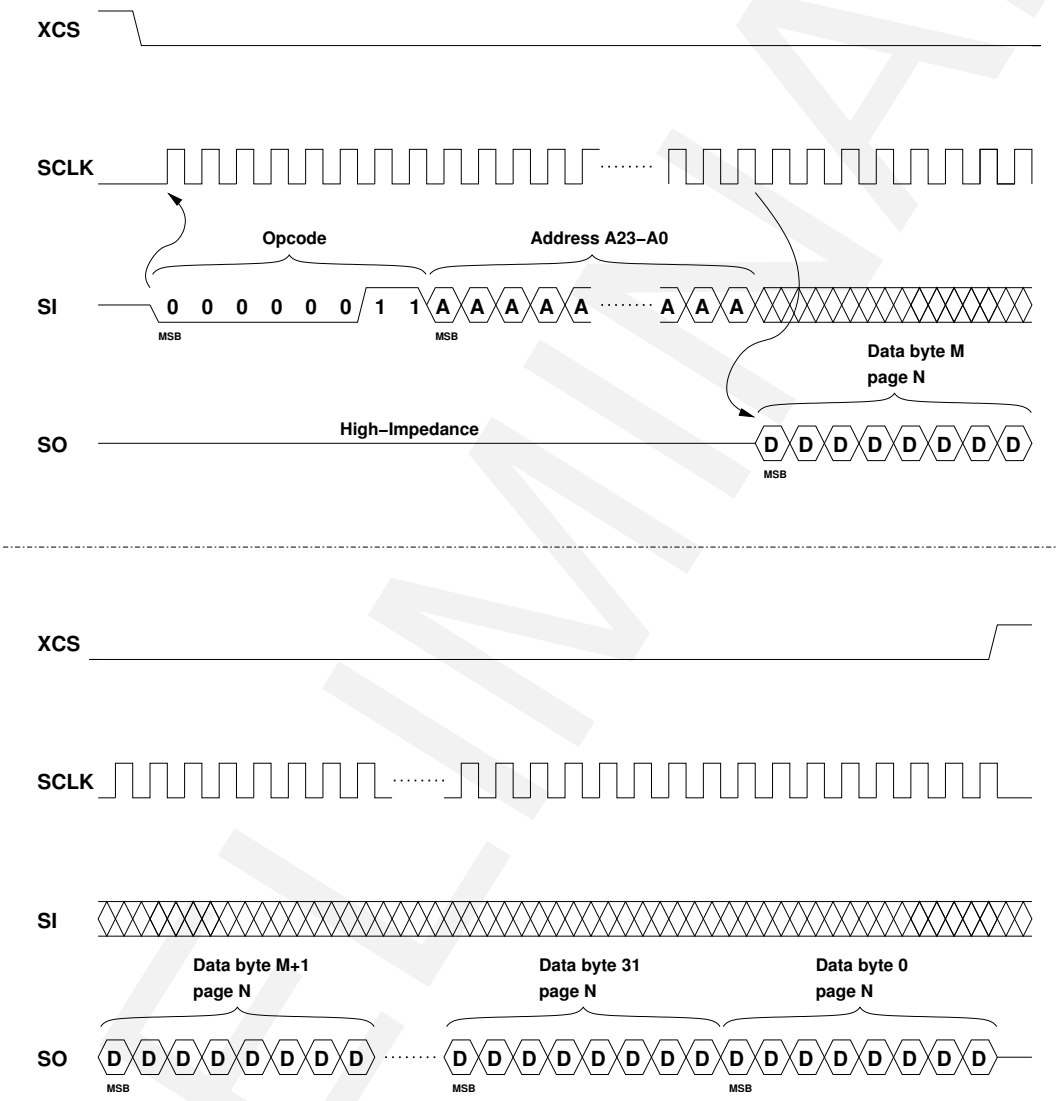


Figure 17: SPI Page read

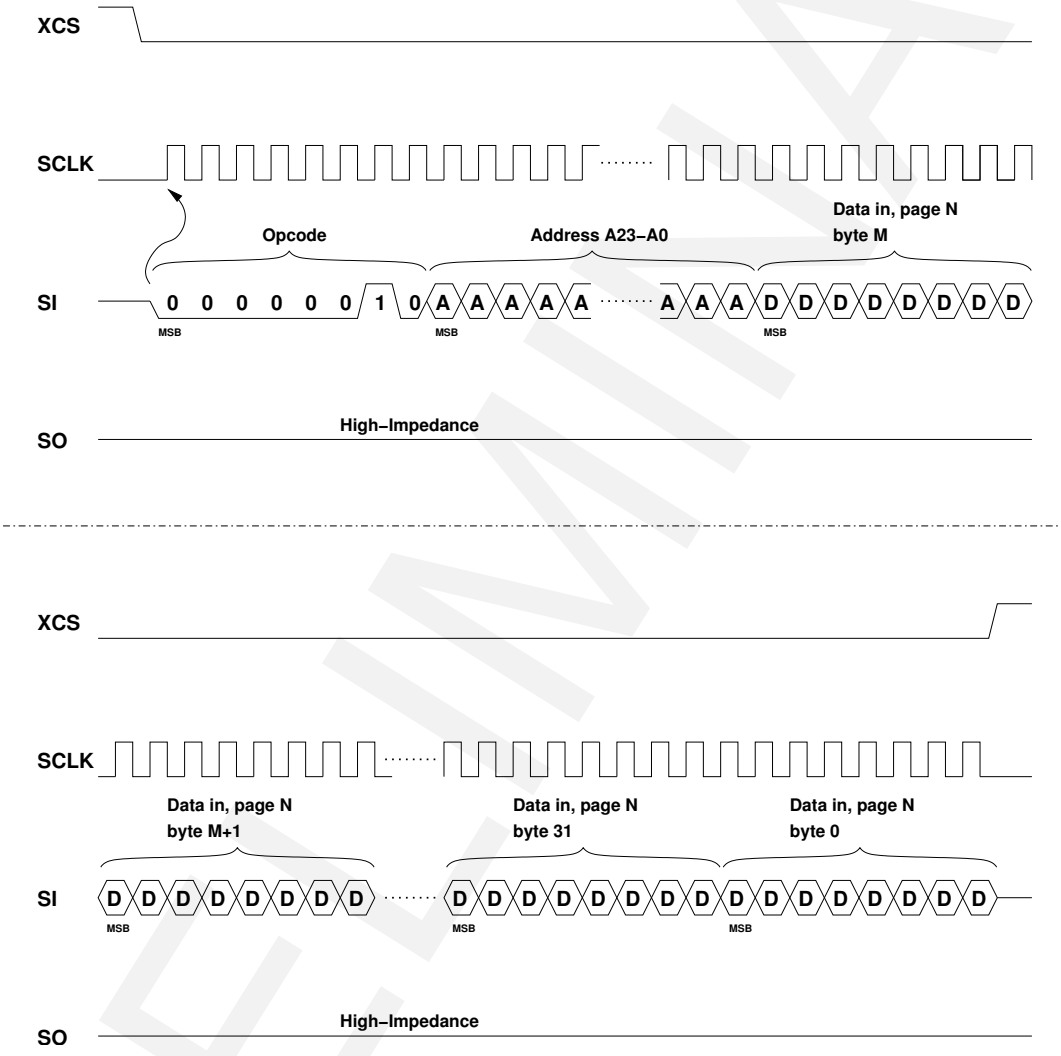


Figure 18: SPI Page write

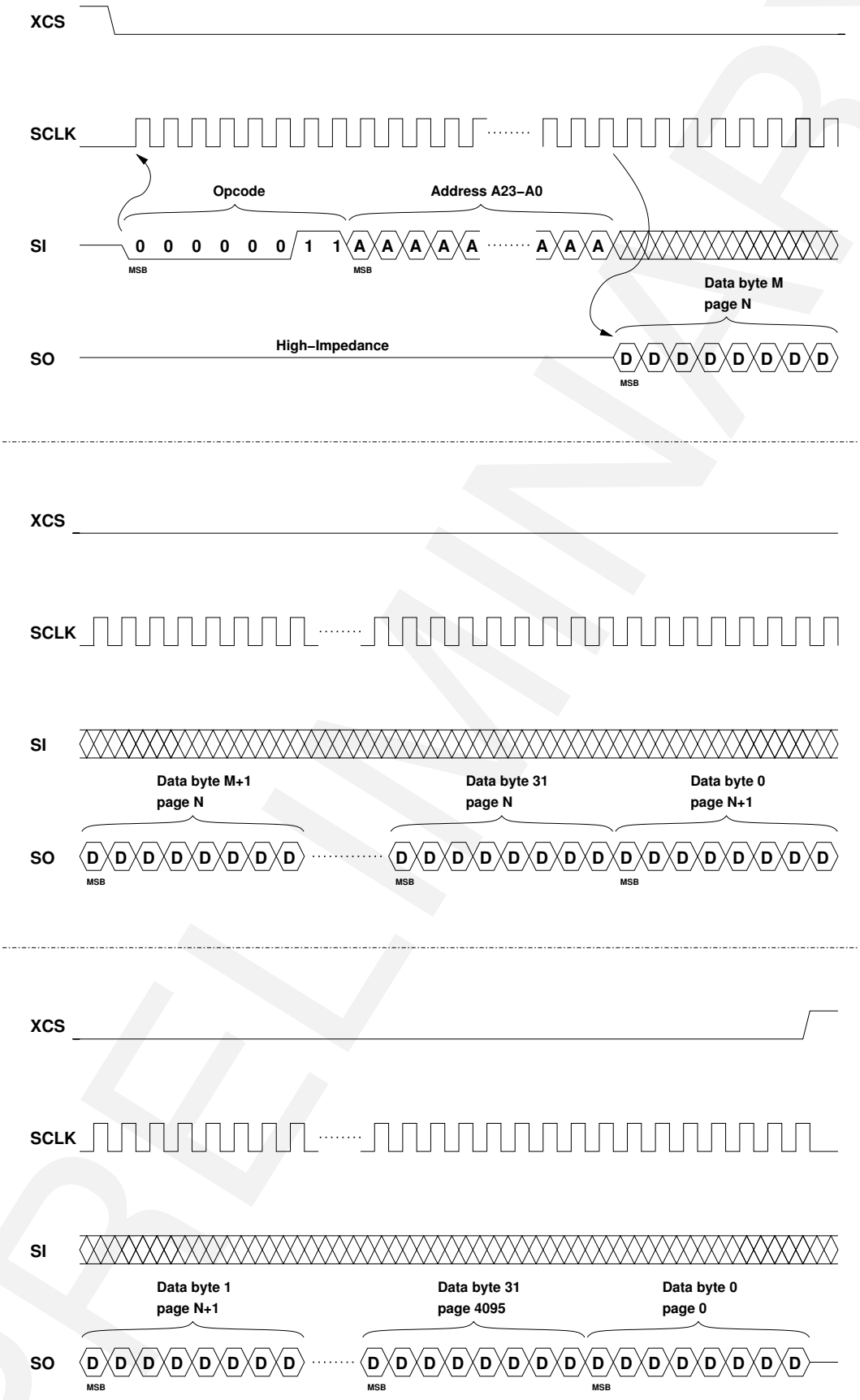


Figure 19: SPI sequential read

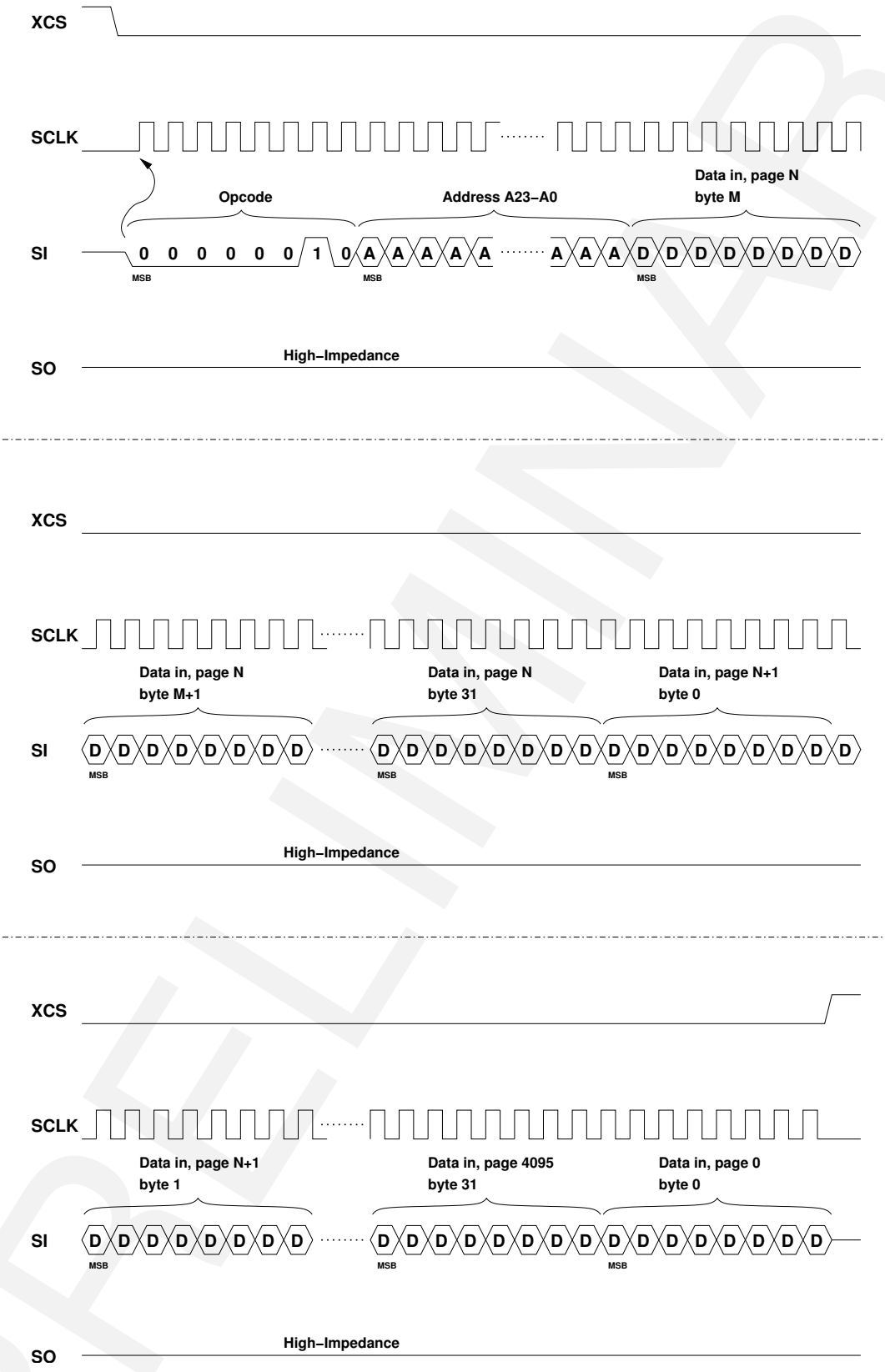


Figure 20: SPI sequential write

6.1.3 Write Protect in Single- and Dual-I/O Modes

In single and dual-I/O modes it is possible to suspend writing of some bits during the write operation. This is done by setting XWP pin to low state when SCLK pin is low. When the XWP pin is low SPI data is not taken into VS23S040D even though SCLK is toggled. The address counter is incremented during this time when SCLK is toggled like normally in write operation. When the XWP pin is set to high during SCLK low state the write operation continues to an updated SRAM address.In Figure 7 is shown XWP timing.

6.1.4 Hold in Single- and Dual-I/O Modes

Hold functionality can be disabled by writing the StSPIH bit of Status register high. After VS23S040D power-up the StSPIH bit is low and Hold function is enabled.

XHOLD pin can be used in single and dual-I/O memory operations. Setting XHOLD low in these modes suspends the operation in progress (SPI read or write). The state of the XHOLD pin can be changed when SCLK is in low state. When XHOLD is low during SPI memory operation the SRAM address counter does not increment even though SCLK is toggled. In read operation the SO output goes to high-impedance state when XHOLD is low. This allows SPI bus to be used by some other device during the VS23S040D memory operation. When the XHOLD pin is set to high again the VS23S040D memory operation continues. In Figures 5 and 6 are shown hold functionality.

6.1.5 Video&Registers Block Selection

It is possible to limit SPI register access to selected Video&Registers Block of VS23S040D by setting bits in Video&Registers Block Selection register. This allows user to write a control command to a selected Video&Registers Block or read a register value from a selected Video&Registers Block. SRAM serial or parallel operations are not affected by this control. Video&Registers Block Selection register writes affect all Video&Registers Blocks of VS23S040D, so that they always have the same value in this register.

6.2 Video Display Controller

The use of Video Display Controller is described in VS23S010D Guide.

6.3 8-Bit Parallel Interface

In parallel mode it is possible to write and read SRAM in the blocks of four bytes (so that the first address of the block has addr mod 4 = 0). 8-bit parallel interface is an alternative interface to SRAM and during its operation SPI has to be inactive. Clock for the parallel interface is generated on-chip by logical and of XRD and XWR pins. XRD and XWR have equal functionality in generating the parallel interface clock and either XRD or XWR can be used to generate clock for read or write. Data pins in this mode are from LSB: SI/IO0, SO/IO1, XWP/IO2, XHOLD/IO3, PIO4, PIO5, PIO6 and PIO7. They are inputs in instruction, address and write phase and outputs in SRAM data read phase.

Parallel interface timing is similar to SPI: Data is always latched in on the rising edge of the clock and always output on the falling edge of the clock. When pins are switched from input to output, there is a delay of one clock cycle before the outputs are driven by VS23S040D.

Additional information considering the usage of interface is given in Chapter 9.

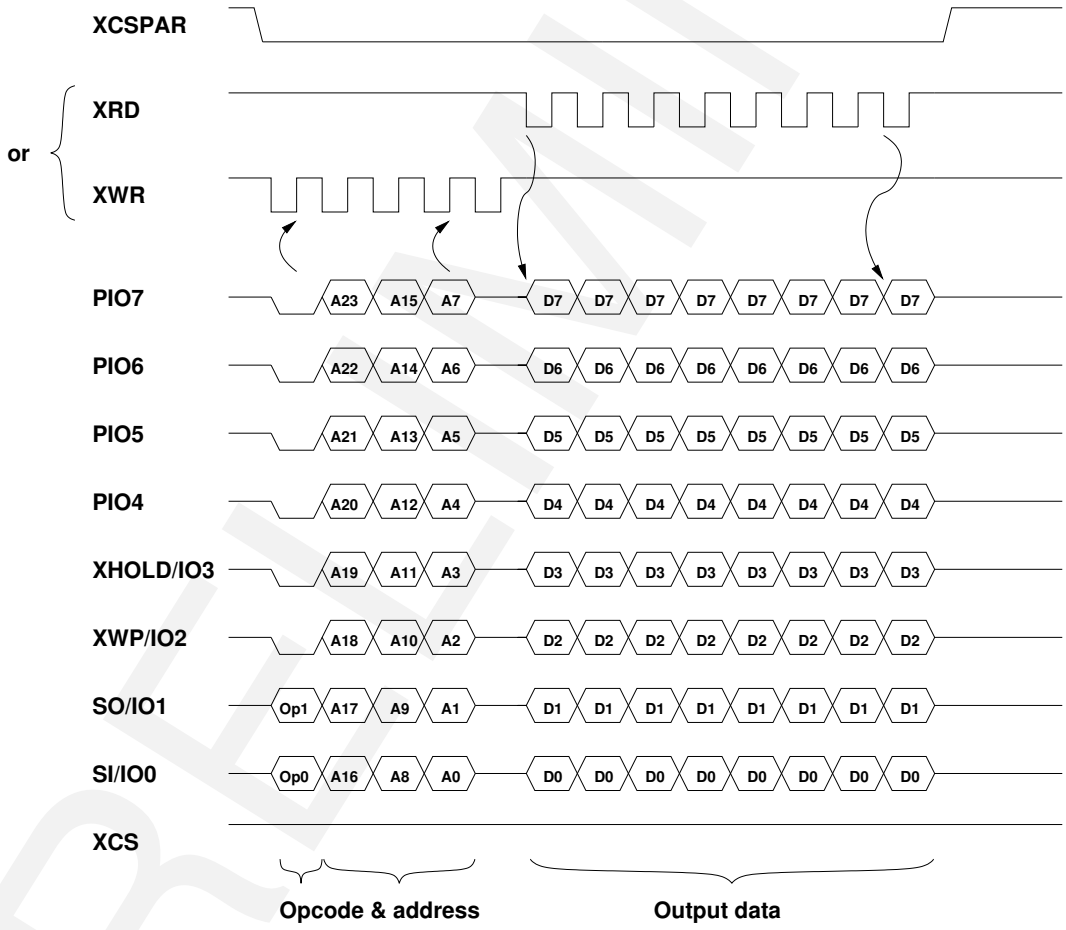


Figure 21: Example of 8-Bit Parallel Interface signals, more detailed timing shown in Chapter 9.

7 SPI Commands and Addressing

A valid SPI instruction or operation is started by first asserting the XCS pin. After that, the host controller clocks out a valid 8-bit opcode on the SPI bus. Following the opcode instruction dependent information (address or data bytes) is sent by the host controller. Address and data are sent MSB first. Operation is ended by deasserting the XCS pin.

Opcodes which are not supported by the VS23S040D are not allowed. Also if XCS is deasserted when the whole byte is not clocked out the operation of the byte in question will be aborted.

Addressing the SRAM of the VS23S040D requires three bytes to be sent, address bits A23-A0. Since the maximum address of one VS23S040D is 7FFFFh the address bits A18 to A0 will be used by device. Address bits A23 to A19 are ignored by the VS23S040D.

Command	Opcode		Address Bytes	Data Bytes
SRAM Read Commands				
Read	03h	0000 0011	3	1+
Dual-Output Read	3Bh	0011 1011	3	1+
Dual-Output Read, Dual Address	BBh	1011 1011	3	1+
Quad-Output Read	6Bh	0110 1011	3	1+
Quad-Output Read, Quad Address	EBh	1110 1011	3	1+
SRAM Write Commands				
Write	02h	0000 0010	3	1+
Dual-Input Write	A2h	1010 0010	3	1+
Dual-Input Write, Dual Address	22h	0010 0010	3	1+
Quad-Input Write	32h	0011 0010	3	1+
Quad-Input Write, Quad Address	B2h	1011 0010	3	1+
Miscellaneous Commands				
Read Status Register	05h	0000 0101	0	1+
Write Status Register	01h	0000 0001	0	1+
Read Manufacturer and Device ID	9Fh	1001 1111	0	1+
Read GPIO Control Register	84h	1000 0100	0	1+
Write GPIO Control Register	82h	1000 0010	0	1+
Read GPIO State Register	86h	1000 0110	0	1+
Read Video&Registers Block Selection	B7h	1011 0111	0	1+
Write Video&Registers Block Selection	B8h	1011 1000	0	1+
Video Display Controller Commands				
Write Picture Start value	28h	0010 1000	0	2
Write Picture End value	29h	0010 1001	0	2
Write Line Length	2Ah	0010 1010	0	2
Write Video Display Controller Control1	2Bh	0010 1011	0	2
Write Picture Index Start address	2Ch	0010 1100	0	2
Write Video Display Controller Control2	2Dh	0010 1101	0	2
Write V Table	2Eh	0010 1110	0	2
Write U Table	2Fh	0010 1111	0	2
Write Program	30h	0011 0000	0	4
Read Current Line value & PLL lock	53h	0101 0011	0	2
Write Block Move Control1	34h	0011 0100	0	5
Write Block Move Control2	35h	0011 0101	0	4
Start Block Move	36h	0011 0110	0	0+

7.1 SPI Read Commands (03h)

The Read command can be used to sequentially read a continuous stream data from the device by providing clock signal once the initial starting address has been specified. The device has on internal address counter that increments or not on every cycle depending on SPI operating mode.

To perform a read operation, XCS must first be asserted and read opcode must be clocked into

device. After the opcode three address bytes are clocked into the device to specify the starting address location of the first byte to read within SRAM.

After address bytes additional SCLK clock cycles will result in data being output on the SO pin. Data is output MSB first. In sequential mode when the last byte (7FFFFh) of the SRAM has been read, the reading will continue from the beginning of the array (00000h).

Deasserting the XCS pin will terminate the read operation and SO pin goes to high-impedance state.

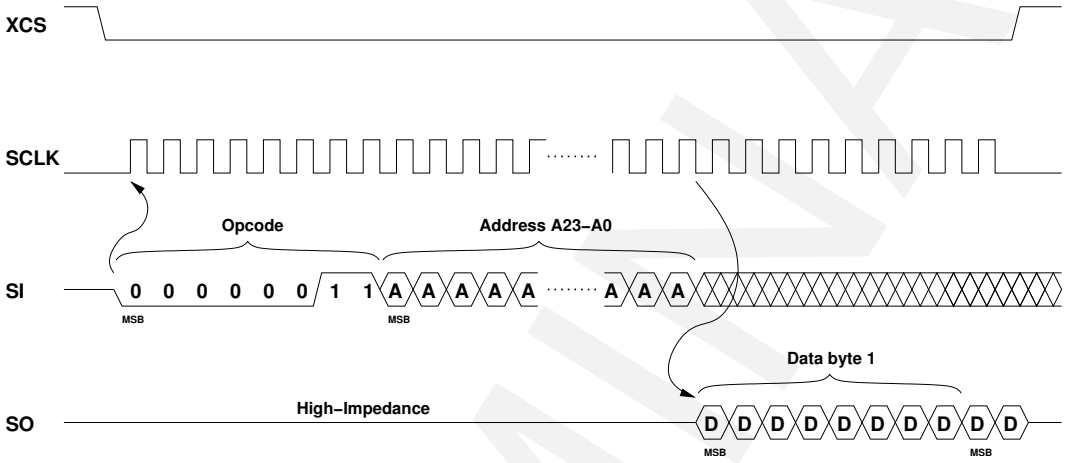


Figure 22: SPI Read

7.1.1 Dual-Output Read (3Bh and BBh)

Dual-Output Read is similar to Read command except that two bits of data are clocked out of the device on every clock cycle.

To perform a Dual-Output Read XCS pin is first asserted. After that opcode 3Bh and three address bytes are sent by the host controller.

After the three address bytes are clocked in, the device will output data on SI/IO0 and SO/IO1 pins. The data is clocked out MSB first and MSB is on pin SO/IO1. During the first clock cycle bit6 will be on SI/IO0 pin, on the next cycle bit5 is on SO/IO1 and bit4 on SI/IO0 and so on. In sequential mode the SRAM addressing will roll over similarly to normal SPI read operation.

Deasserting the XCS pin will terminate the read operation and SI/IO0 and SO/IO1 pins go to high-impedance state.

Dual-Output, Dual Address Read is similar to Dual-Output Read command except that two bits of address are clocked in the device on every clock cycle.

To perform a Dual-Output, Dual Address Read XCS pin is first asserted. After that opcode BBh is sent in one bit mode and three address bytes are sent in dual I/O mode by the host controller

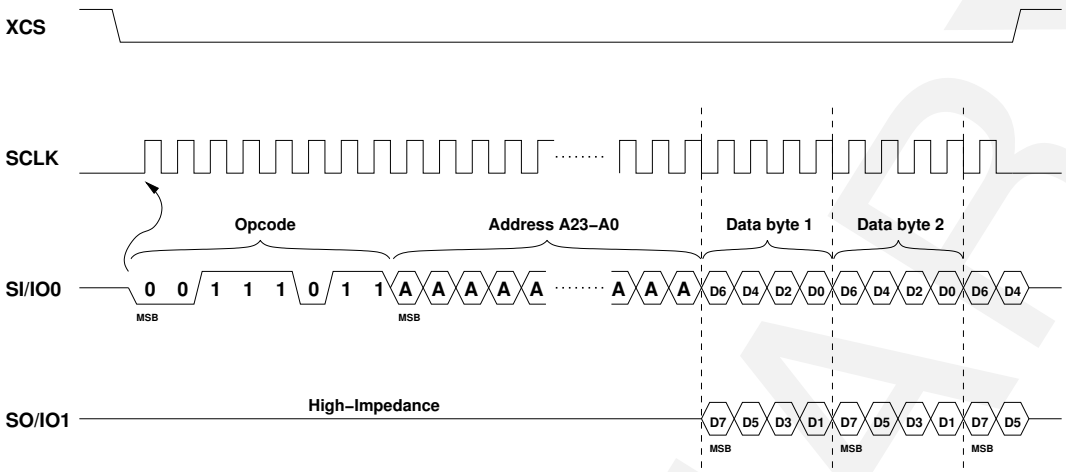


Figure 23: SPI Dual-Output Read

to SI/IO0 and SO/IO1 pins.

After the three address bytes are clocked in, there is a dummy byte cycle. After that the device will output data on SI/IO0 and SO/IO1 pins. The rest of the operation is similar to Dual-Output Read.

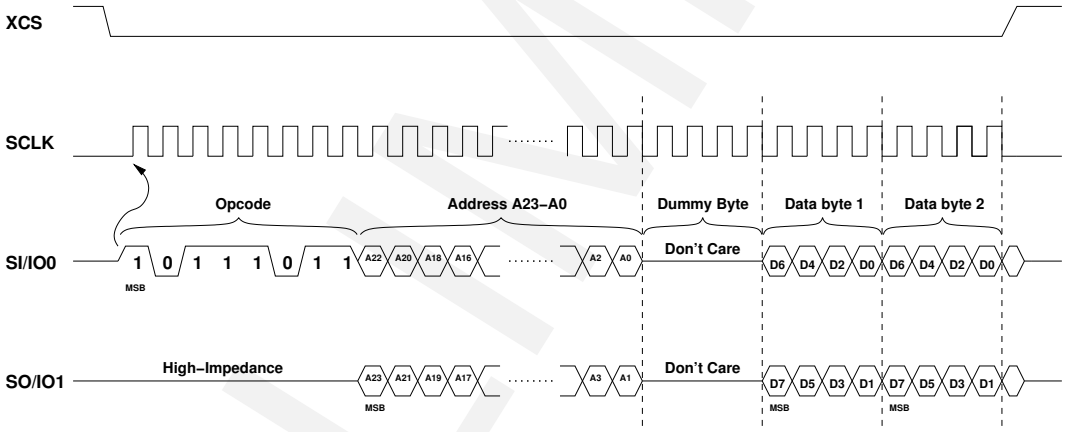


Figure 24: SPI Dual-Output Read, Dual Address

7.1.2 Quad-Output Read (6Bh and EBh)

Quad-Output Read is similar to Read command except that four bits of data are clocked out of the device on every clock cycle.

To perform a Quad-Output Read XCS pin is first asserted. After that opcode 6Bh and three address bytes are sent by the host controller.

After the three address bytes are clocked in, the device will output data on SI/IO0, SO/IO1, XWP/IO2 and XHOLD/IO3 pins. The data is clocked out MSB first and MSB is on pin XHOLD/IO3. During the first clock cycle bit6 will be on XWP/IO2 pin, bit5 on pin SO/IO1 and bit4 on SI/IO0,

on the next cycle bit3 is on XHOLD/IO3 and bit2 on XWP/IO2 and so on. In sequential mode the SRAM addressing will roll over similarly to normal SPI read operation.

Deasserting the XCS pin will terminate the read operation and SI/IO0, SO/IO1, XWP/IO2 and XHOLD/IO3 pins go to high-impedance state.

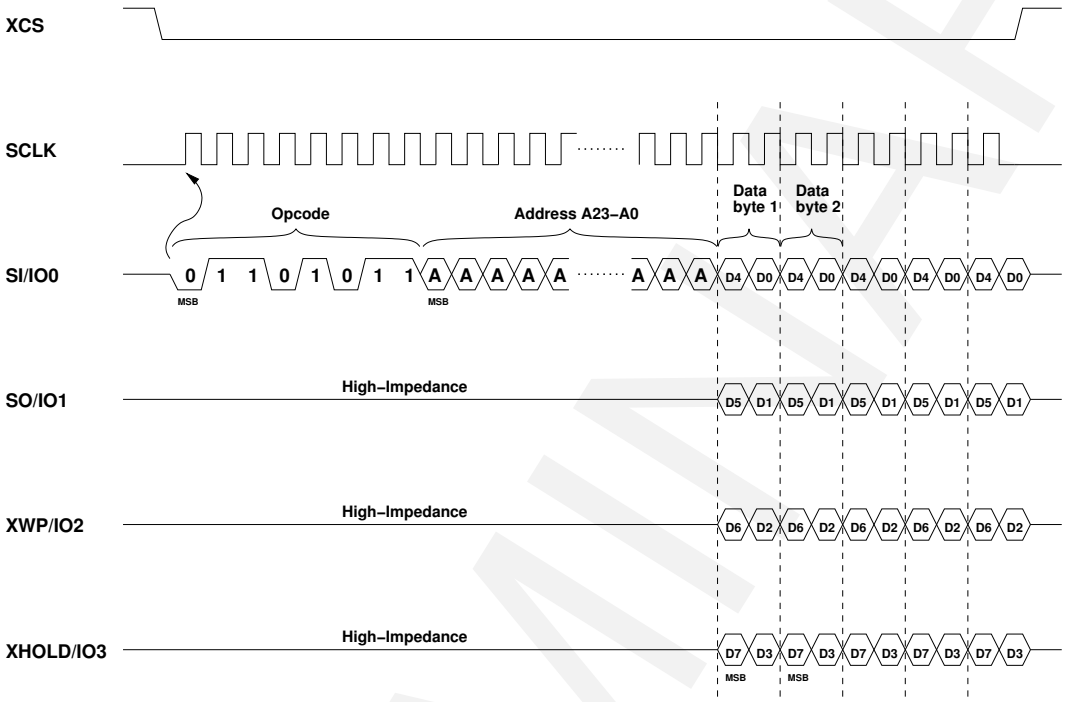


Figure 25: SPI Quad-Output Read

Quad-Output, Quad Address Read is similar to Quad-Output Read command except that four bits of address are clocked in the device on every clock cycle.

To perform a Quad-Output, Quad Address Read XCS pin is first asserted. After that opcode EBh is sent in one bit mode and three address bytes are sent in quad I/O mode by the host controller to SI/IO0, SO/IO1, XWP/IO2 and XHOLD/IO3 pins.

After the three address bytes are clocked in, there is a dummy byte cycle. After that the device will output data on SI/IO0, SO/IO1, XWP/IO2 and XHOLD/IO3 pins. The rest of the operation is similar to Quad-Output Read.

7.2 SPI Write Commands (02h)

Prior to writing the device must be selected by bringing XCS pin low. Once the device is selected the Write command can be started by issuing a Write instruction (opcode 02h) followed by a 23-bit address. If the device works in sequential mode (set by Status Register write) then after the initial data byte additional bytes can be clocked into device. The internal address pointer is automatically incremented when needed depending on operating mode. In sequential mode when the internal address pointer reaches its maximum value (7FFFFh) it rolls over

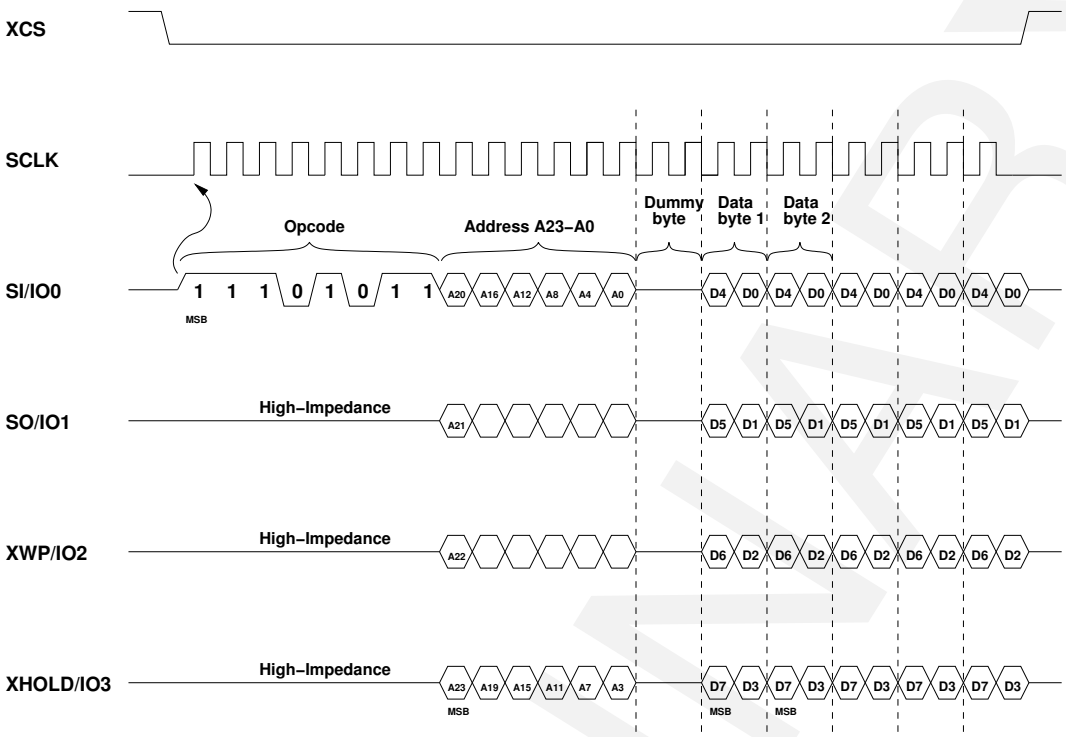


Figure 26: SPI Quad-Output Read, Quad Address

to 00000h. This allows the operation to continue indefinitely, however, previous data will be overwritten.

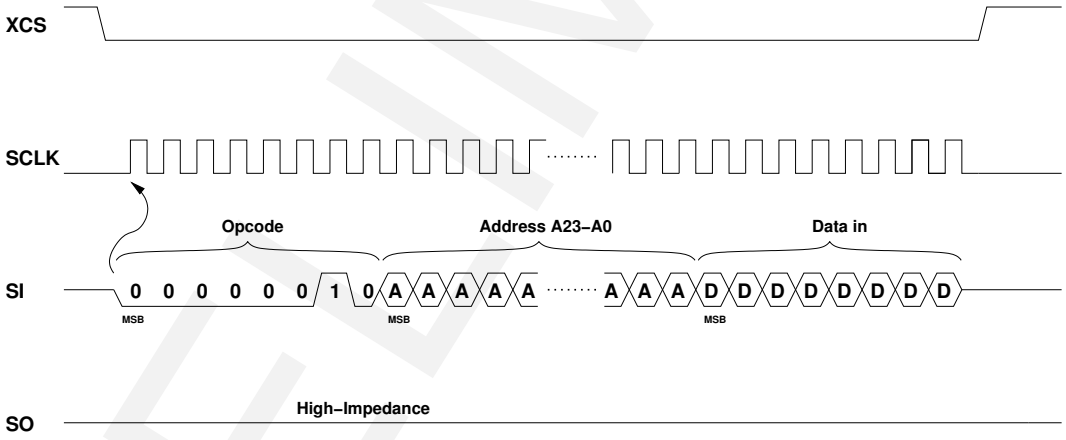


Figure 27: SPI Write

7.2.1 Dual-Input Write (A2h and 22h)

Dual-Input Write command is similar to Write command except that two bits of data are clocked in the device on every clock cycle and opcode is A2h.

Dual-Input, Dual Address Write command is similar to Dual-Input Write command except that two bits of address are clocked in the device on every clock cycle and opcode is 22h.

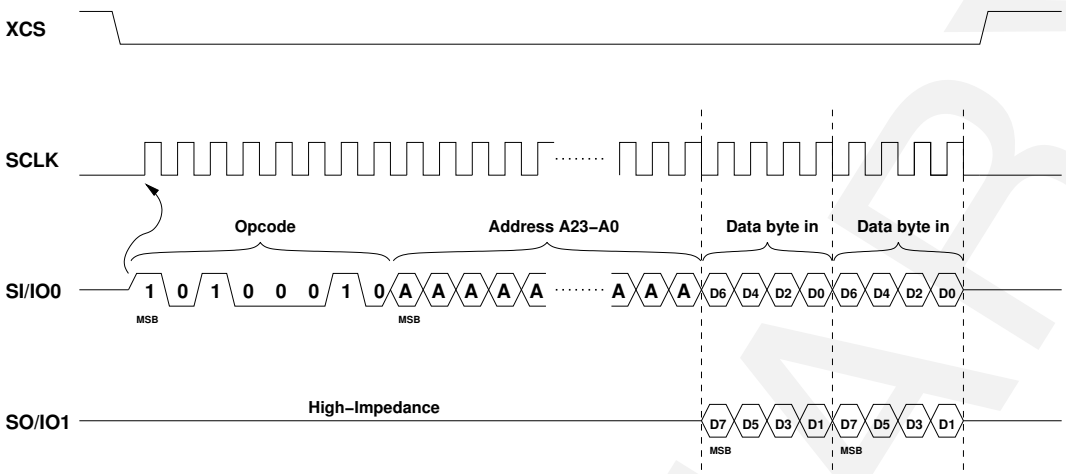


Figure 28: SPI Dual-Input Write

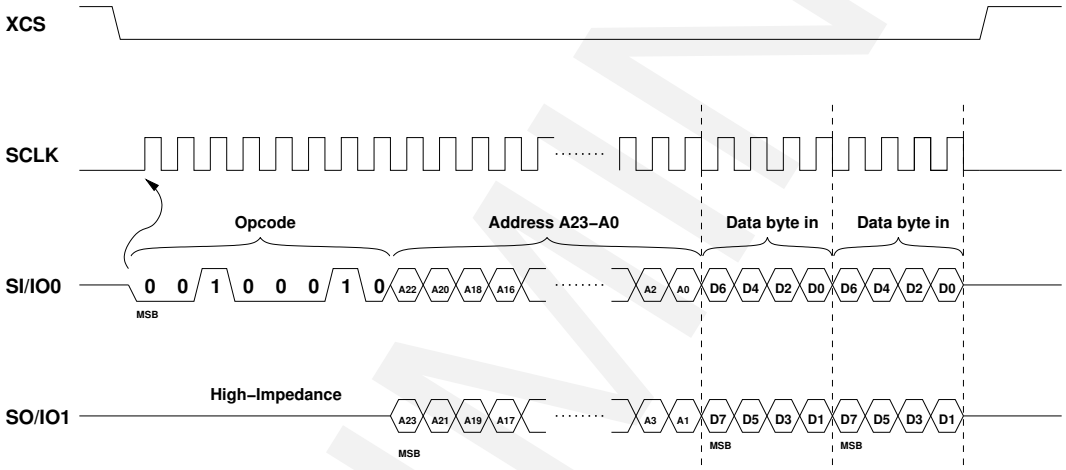


Figure 29: SPI Dual-Input, Dual Address Write

7.2.2 Quad-Input Write (32h and B2h)

Quad-Input Write command is similar to Write command except that four bits of data are clocked in the device on every clock cycle and opcode is 32h.

Quad-Input, Quad Address Write command is similar to Quad-Input Write command except that four bits of address are clocked in the device on every clock cycle and opcode is B2h.

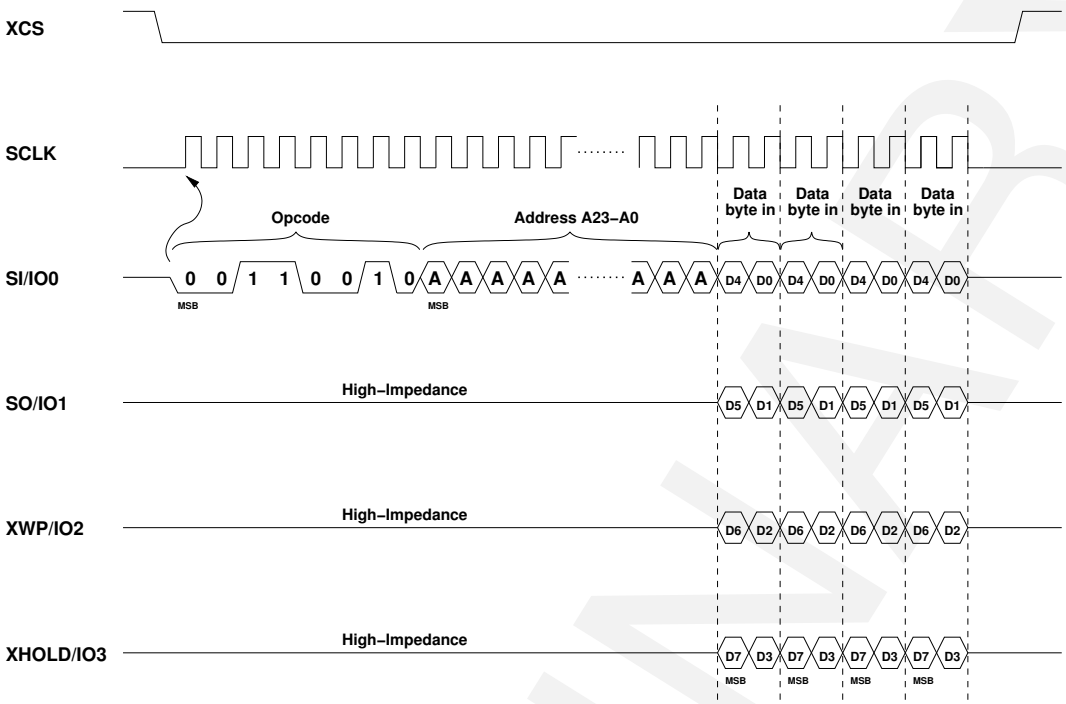


Figure 30: SPI Quad-Input Write

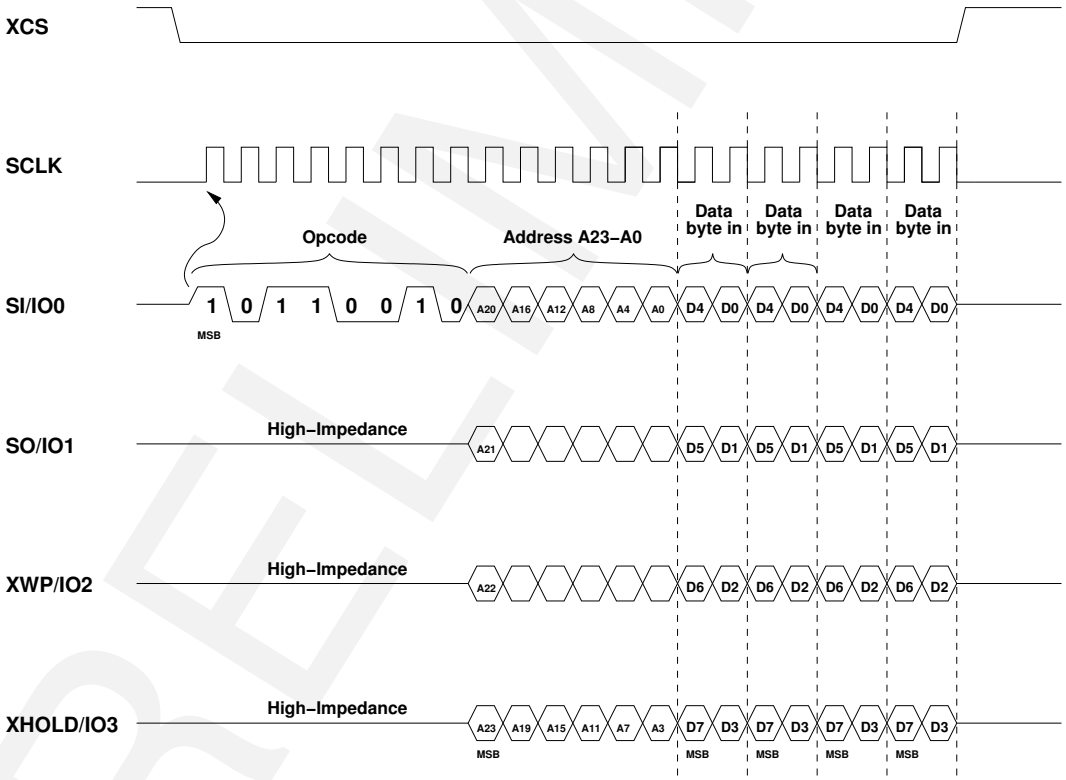


Figure 31: SPI Quad-Input, Quad Address Write

7.3 SPI Miscellaneous Commands

These commands are affected by the DisROpsn control bits of the Video&Registers Block Selection register. It is possible to write register of one, two, three or four Video&Registers Blocks with one SPI command depending on the value of the Video&Registers Block Selection register. Reading a register value can be done similarly, but if the registers of different Video&Registers Blocks have different values, the output data can have a wrong value. So, a register of a single Video&Registers Block is advised to be read. Video&Registers Block Selection register is not affected by these bits. When that register is written all four Video&Registers Block Selection registers are set to same value. Also when Video&Registers Block Selection register is read the same value is received from all four Video&Registers Blocks.

7.3.1 Read Status Register (05h)

The Read Status command is started by asserting XCS pin. After that the host controller sends the opcode, 05h. The device responds by clocking out a byte wide value of Status register. When XCS pin is deasserted, the clocking out of the register is ended and SO pin goes to high-impedance state.

Output Bits	Name		Type	Description	
7-6	StSPIMn	SPI Mode	RW	0 0 0 1 1 0 1 1	Byte Mode (Default) Sequential Mode Page Mode Reserved
5	Reserved	Reserved	RW	0	Default
4	StFastWV	SPI Fast Write in Video Mode	RW RW	0 1	Normal write (Default) Fast write
3-1	StUsern	User Bits	RW		User Bits
0	StSPIH	SPI Hold Function	RW	0 1	Hold (Default) No Hold

StSPIMn These bits indicate the operating mode of the SPI of the VS23S040D. StSPIMn bits affect the operation in all SPI SRAM read and write modes.

Reserved This bit is reserved. It has to be low always for correct functionality of the VS23S040D.

StFastWV StFastWV bit enables fast write mode when video generation is enabled. In fast write mode it is possible to write up to six times the amount of data compared to normal mode.

There are two limitations. The modulo-4 of the start address has to be zero. Otherwise the SRAM data below start address to address, which is equally divisible by four is set to 00h.

Also the modulo-4 of last address has to equal three in fast write mode. If modulo-4 of the last address is something else, then the last 1 to 3 bytes are not written to SRAM. Fast write mode is only for SPI write operations when Video Display Controller is enabled.

StUsern StUsern bits are user assignable and have no effect to operation on VS23S040D. Default value is low.

StSPIH StSPIH enables Hold functionality in Single and Dual mode SPI operations. Default value is “0” which means that Hold functionality is enabled.

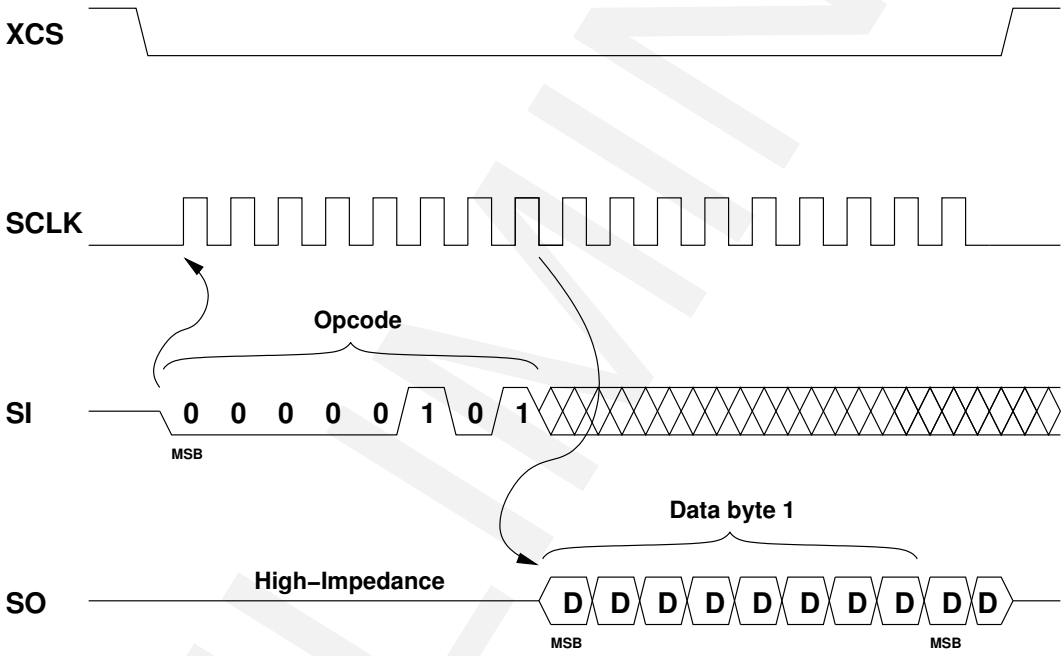


Figure 32: SPI Read Status Register

7.3.2 Write Status Register (01h)

To write the GPIO Control register XCS pin must be first asserted and opcode 01h clocked into the device. After that byte-wide value is clocked in the device via SI pin. The value is input MSB (bit 7) first. The state of the Status Register bits is changed according to the received byte after the SCLK goes low. Note, that bit 5 has to be low always.

Write Status Register Format							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
StSPIM1	StSPIM0	Reserved, ”0”	StFastWV	StUser2	StUser1	StUser0	StSPIH

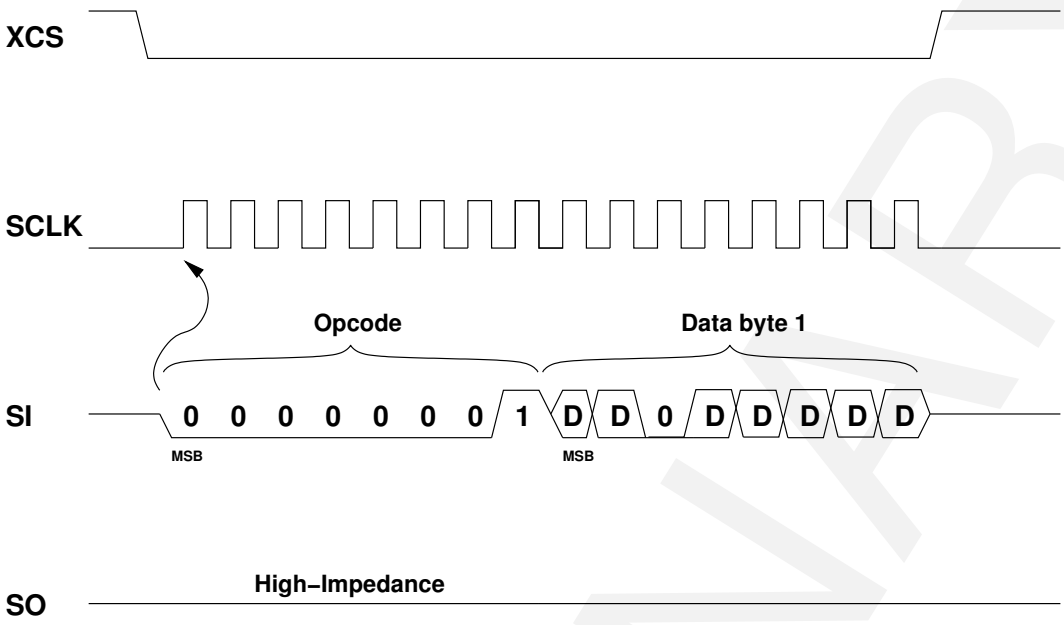


Figure 33: SPI Write Status Register

7.3.3 Read Manufacturer and Device ID (9Fh)

The Read Manufacturer and Device ID command is started by asserting XCS pin. After that the host controller sends the opcode, 9Fh. The device responds by clocking out a byte wide constant, value 2Bh. The two lowest bits of the second byte inform the amount of Video&Registers Blocks and also the amount of SRAM. The second byte is always 03h in VS23S040D. When XCS pin is deasserted, the clocking out of the data is ended and SO pin goes to high-impedance state.

Note, Manufacturer and Device ID is read-only register.

Bits	Name		Type	Description	
15-8	ID	Manufacturer and Device ID	R	2Bh	ID (default)
7-2		Don't care	R	0	default
1-0	Conf	Device configuration	R	11	Four Video&Registers Blocks, 4 Mbit SRAM

7.3.4 Read GPIO Control Register (84h)

The Read GPIO Control Register command is started by asserting XCS pin. After that the host controller sends the opcode, 84h. The device responds by clocking out a byte wide value. When XCS pin is deasserted, the clocking out of the register value is ended and SO pin goes to high-impedance state.

If GPIOs of several Video&Registers Blocks are configured as outputs, then it is very strongly recommended that the output state is same in all dies. Otherwise there is a short-circuit current which may cause device malfunction.

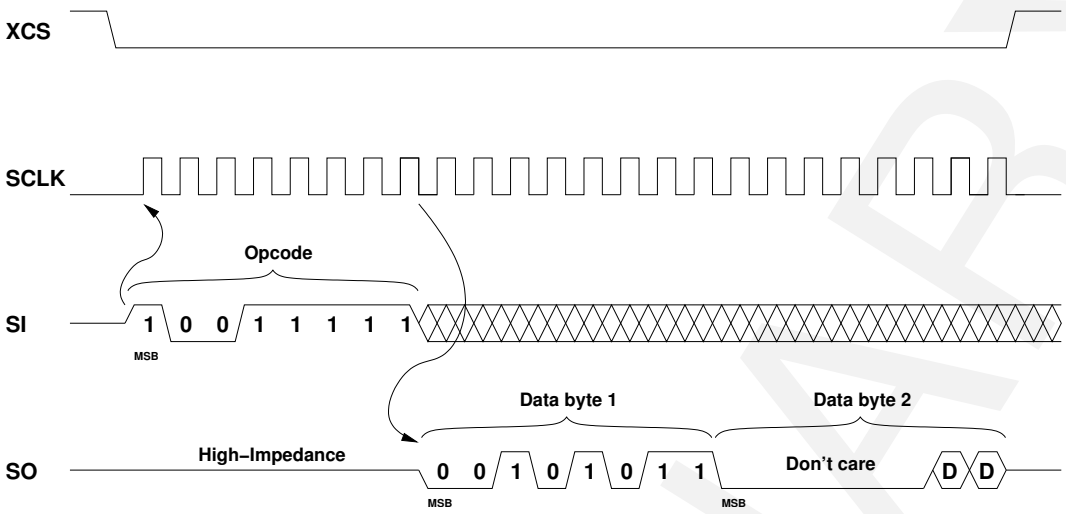


Figure 34: SPI Read Manufacturer and Device ID

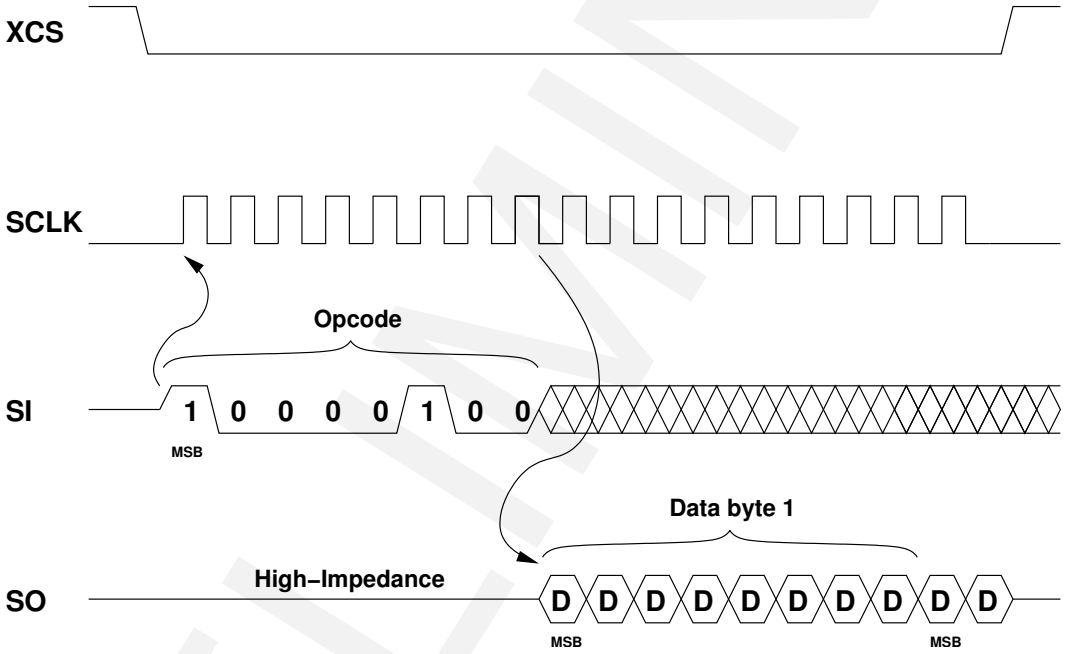


Figure 35: SPI Read GPIO Control

Bits	Name		Type	Description	
7-4	PIOnD	PIO7-4 Direction	RW	0 1	Input (default) Output
3-0	PIOnO	PIO7-4 Output State	RW	0 1	Low (default) High

PIOnD PIOnD bits set the direction of PIO7-4 pins, when 8-bit parallel interface is not used. Default value “0” sets a PIO as input. Bit 7 sets PIO7 direction, bit 6 PIO6 direction and so on.

High value “1” sets the PIO as output with a value set in PIOnO bits.

PIOnO PIOnO bits set the PIO7-4 output state. Default is “0”, which sets the state low. Bit 3 sets PIO7 output state, bit 3 PIO6 output state etc.

High value “1” sets the corresponding PIO state to high.

Note, that 8-bit parallel interface overrides GPIO functionality of PIO7-4.

7.3.5 Write GPIO Control Register (82h)

To write the GPIO Control register XCS pin must be first asserted and opcode 82h clocked into the device. After that byte-wide value is clocked in the device via SI pin. The value is input MSB (bit 7) first. The state of the PIO7-4 pins is changed according to the received byte after the SCLK goes low.

If GPIOs of several Video&Registers Blocks are configured as outputs, then it is very strongly recommended that the output state is same in all dies. Otherwise there is a short-circuit current which may cause device malfunction.

Write GPIO Control Register Format							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIO7D	PIO6D	PIO5D	PIO4D	PIO7O	PIO6O	PIO5O	PIO4O

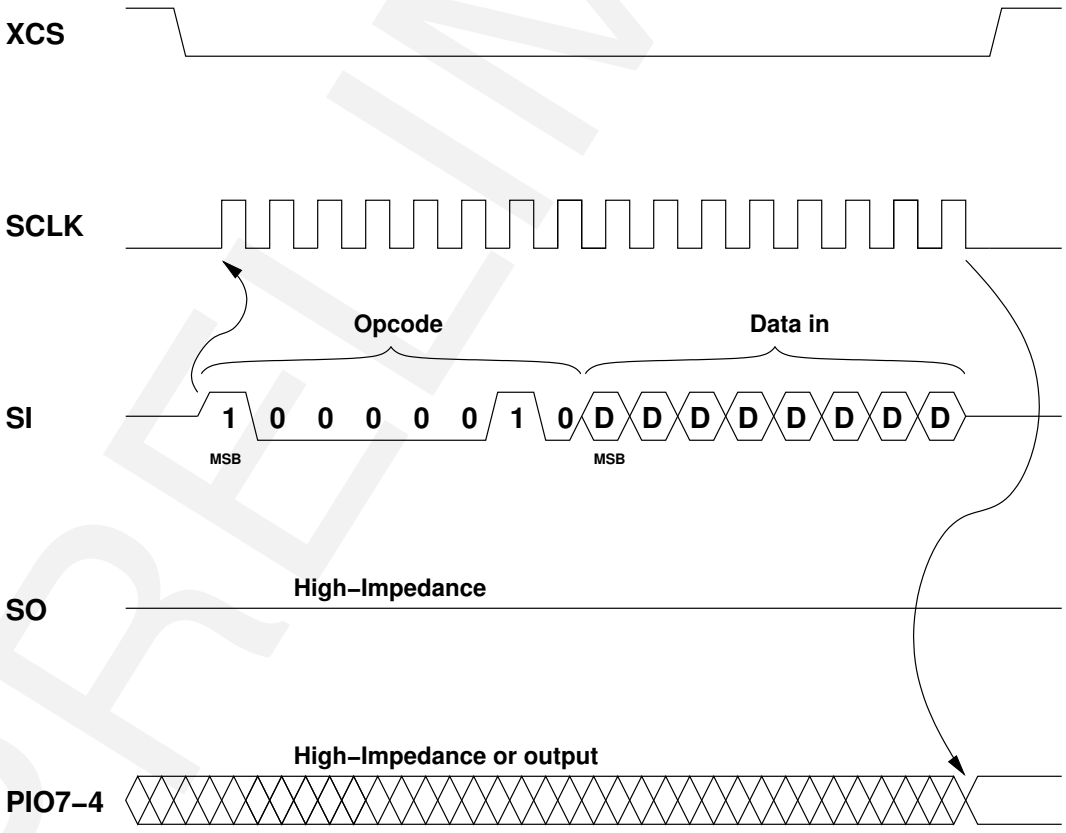


Figure 36: SPI Write GPIO Control

7.3.6 Read GPIO State Register (86h)

The Read GPIO State Register command is started by asserting XCS pin. After that the host controller sends the opcode, 86h. The device responds by clocking out a byte wide value. When XCS pin is deasserted, the clocking out of the register value is ended and SO pin goes to high-impedance state.

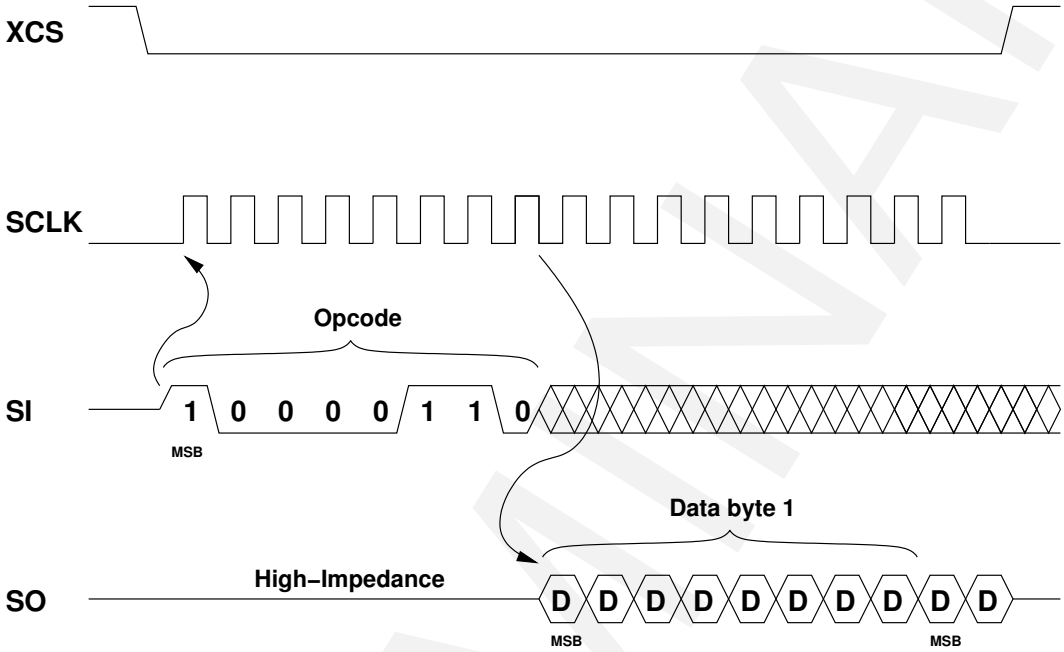


Figure 37: SPI Read GPIO State

Output Bit	GPIO State Description
7	PIO7 logic state
6	PIO6 logic state
5	PIO5 logic state
4	PIO4 logic state
3	XHOLD logic state
2	XWP logic state
1	PLL lock
0	Video Generator block move active

7.3.7 Read Video&Registers Block Selection Register (B7h)

The read Video&Registers Block Selection Register command is started by asserting XCS pin. After that the host controller sends the opcode, B7h. The device responds by clocking out a byte wide value. When XCS pin is deasserted, the clocking out of the register value is ended and SO pin goes to high-impedance state.

The Video&Registers Block Selection register operations are not affected by DisROpsn bits. A write to Video&Registers Block Selection register sets the register value in all four Video&Registers

Blocks of the VS23S040D.

Bits	Name		Type	Description	
7-4	Reserved		RW	0000	Always 00h (default)
3-0	DisROpsn	Disable SPI register operations	RW	0000	Reg ops enabled for all Video&Registers Blocks (default)
				0001	Reg ops disabled for 1st Video&Registers Block
				0010	Reg ops disabled for 2nd Video&Registers Block
				0100	Reg ops disabled for 3rd Video&Registers Block
				1000	Reg ops disabled for 4th Video&Registers Block
				...	
				1111	Reg ops disabled for all Video&Registers Blocks

DisROpsn In Video&Registers Block Selection setup DisROpsn bits are used to control the SPI writes to and reads from VS23S040D registers. SRAM operations and Video&Registers Block Selection register accesses are not affected by this control.

The low bit value “0” enables SPI writes to and reads from registers of particular Video&Registers Block of VSR. The high bit value “1” disables the operations.

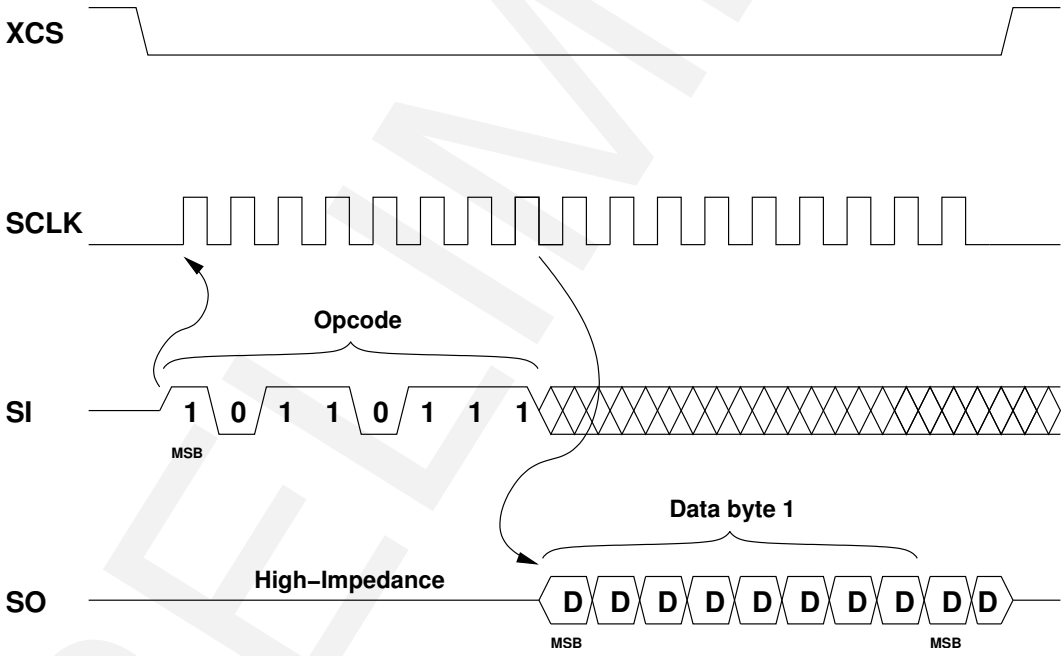


Figure 38: SPI Read Video&Registers Block Selection

7.3.8 Write Video&Registers Block Selection Register (B8h)

To write the Video&Registers Block Selection register XCS pin must be first asserted and op-code B8h clocked into the device. After that byte-wide value is clocked in the device via SI pin.

The value is input MSB (bit 7) first. The state of the Video&Registers Block Selection register bits is changed according to the received byte after the SCLK goes low.

The Video&Registers Block Selection register operations are not affected by DisROpsn bits. A write to Video&Registers Block Selection register sets the register value in all four Video&Registers Block of the VS23S040D.

Write Video&Registers Block Selection Register Format							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved, 00h				DisROps3	DisROps2	DisROps1	DisROps0

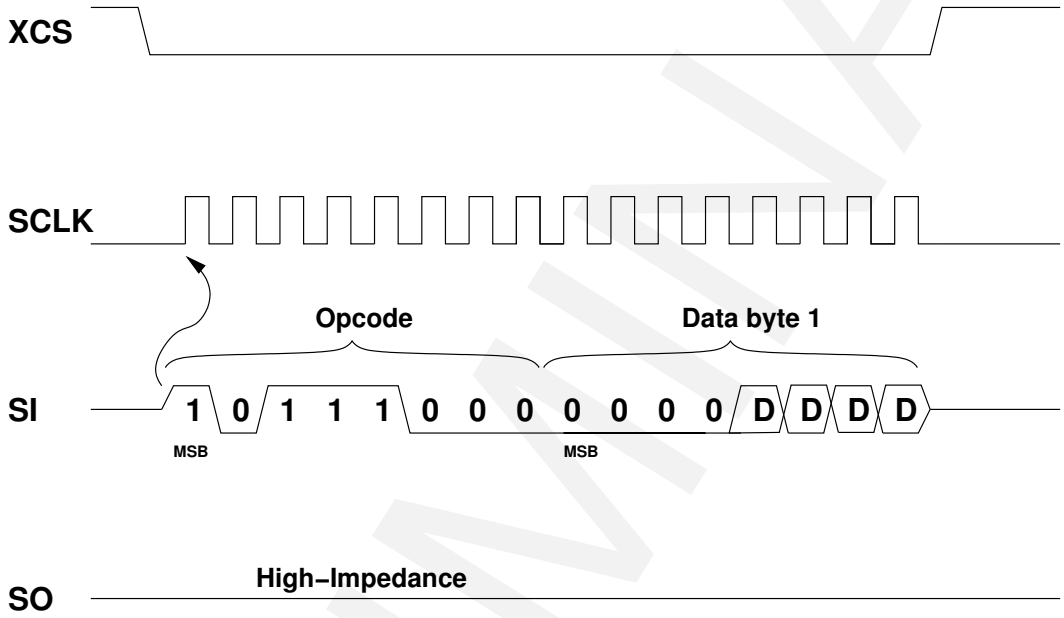


Figure 39: SPI Write Video&Registers Block Selection

8 Video Display Controller Commands

These commands are affected by the DisROpsn control bits of the Video&Registers Block Selection register. It is possible to write register of one, two, three or four Video&Registers Blocks with one SPI command depending on the value of the Video&Registers Block Selection register. Reading a register value can be done similarly, but if the registers of different Video&Registers Blocks have different values, the output data can have a wrong value. So, generally a register of a single Video&Registers Block is advised to be read.

8.1 Write Picture Start (28h)

Picture Start value defines the pixel position where the normal line starts. The position is defined by CSClk cycles (i.e. color subcarrier cycles) from the start of the line. The fixed 1.25 CSClk (10 VClk) cycles long sync level at the beginning of each line is additional to given Picture Start value. Note, that Picture Start value has to be less than Line Length divided by 8. The recommended minimum value of Picture Start is 7.

To write the Picture Start register XCS pin must be first asserted and opcode 28h clocked into the device. After that two byte value is clocked in the device via SI pin. The two byte value is input MSB (bit 15) first. The register value is 12 bits (11:0) wide, so bits 15 to 12 are don't cares. When XCS pin is deasserted the Picture Start register will be updated.

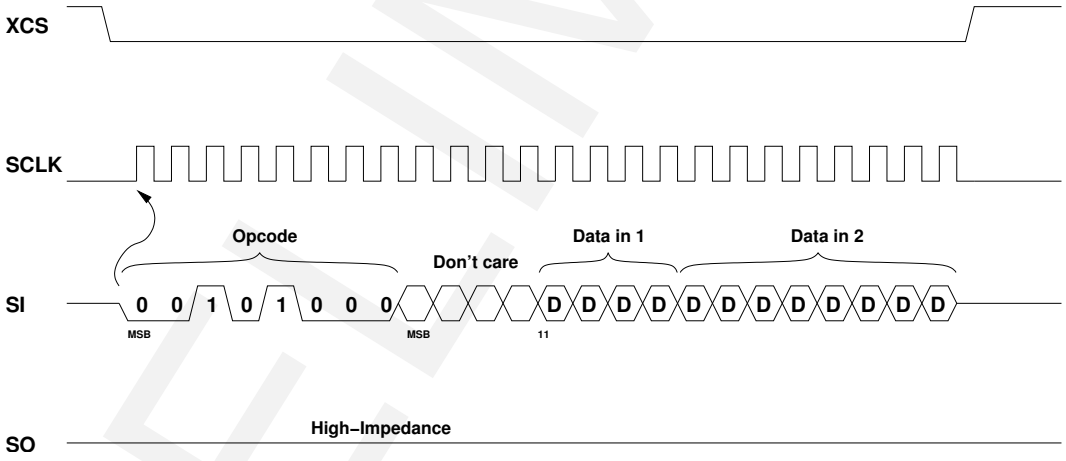


Figure 40: SPI Write Picture Start

8.2 Write Picture End (29h)

Picture End value defines the pixel position where the protoline starts after normal line. The position is defined by CSClk cycles (i.e. color subcarrier cycles) from the start of the line. The fixed 1.25 CSClk cycles long sync level at the beginning of each line is additional to given Picture End value. Note, that Picture End value has to be less than or equal to Line Length divided by 8. Also Picture End value has to be larger than Picture Start value.

To write the Picture End register XCS pin must be first asserted and opcode 29h clocked into the device. After that two byte value is clocked in the device via SI pin. The two byte value is input MSB (bit 15) first. The register value is 12 bits (11:0) wide, so bits 15 to 12 are don't cares. When XCS pin is deasserted the Picture End register will be updated.

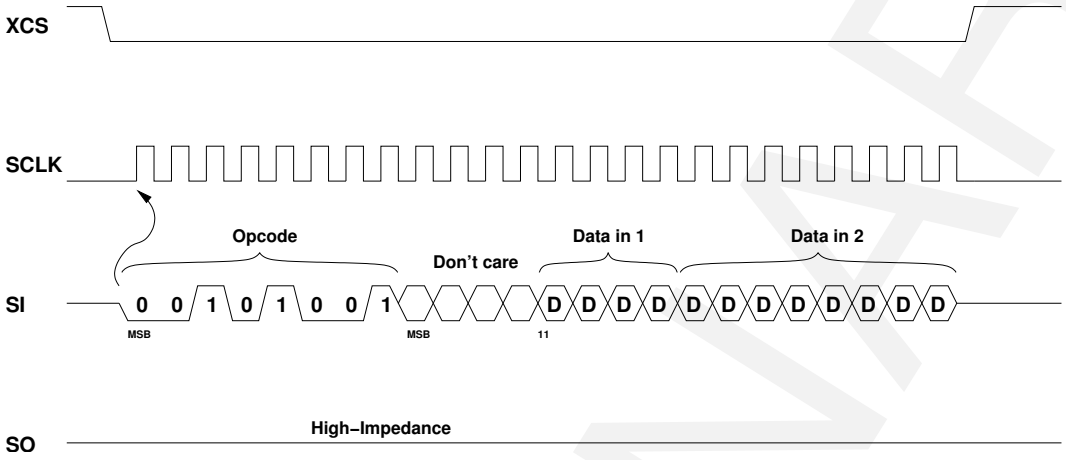


Figure 41: SPI Write Picture End

8.3 Write Line Length (2Ah)

Line Length value defines the length of a single line. The Length is given in VClk cycles. The fixed 10 VClk cycles long sync level at the beginning of each line is additional to given Line Length value.

To write the Line Length register XCS pin must be first asserted and opcode 2Ah clocked into the device. After that two byte value is clocked in the device via SI pin. The two byte value is input MSB (bit 15) first. Bit 15 (VGP bit) of the register is used for selecting the digital 4-bit control output to PIO pins. The Line Length value is 12 bits (11:0) wide, so bits 14 to 12 are don't cares. When XCS pin is deasserted the Line Length register will be updated.

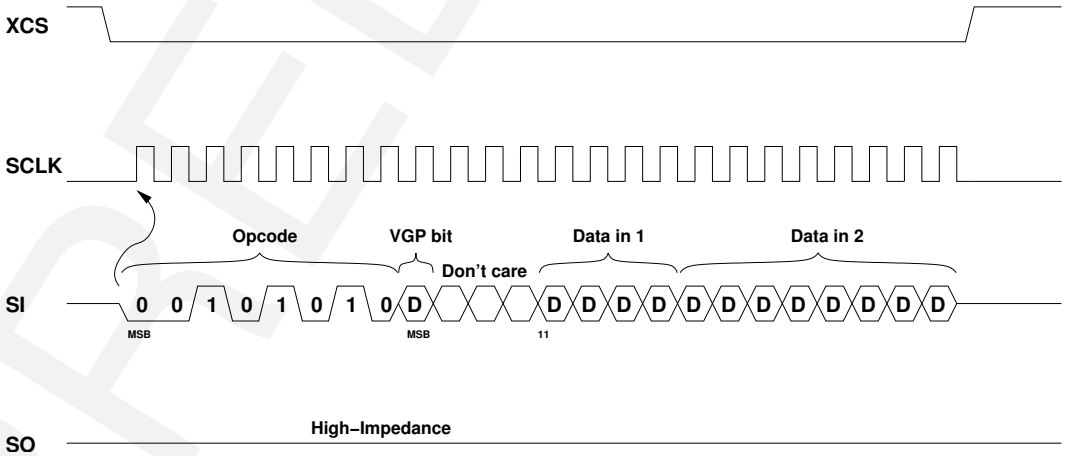


Figure 42: SPI Write Line Length

In Direct DAC mode the Line Length is used to define the buffer length of DAC data buffer. The

actual DAC data buffer length is the register value increased by one, i.e. the range is from 1 to 4096.

8.4 Write Video Display Controller Control1 (2Bh)

To write the Video Display Controller Control1 register XCS pin must be first asserted and opcode 2Bh clocked into the device. After that two byte value is clocked in the device via SI pin. The two byte value is input MSB (bit 15) first. When XCS pin is deasserted the Video Display Controller Control1 register will be updated.

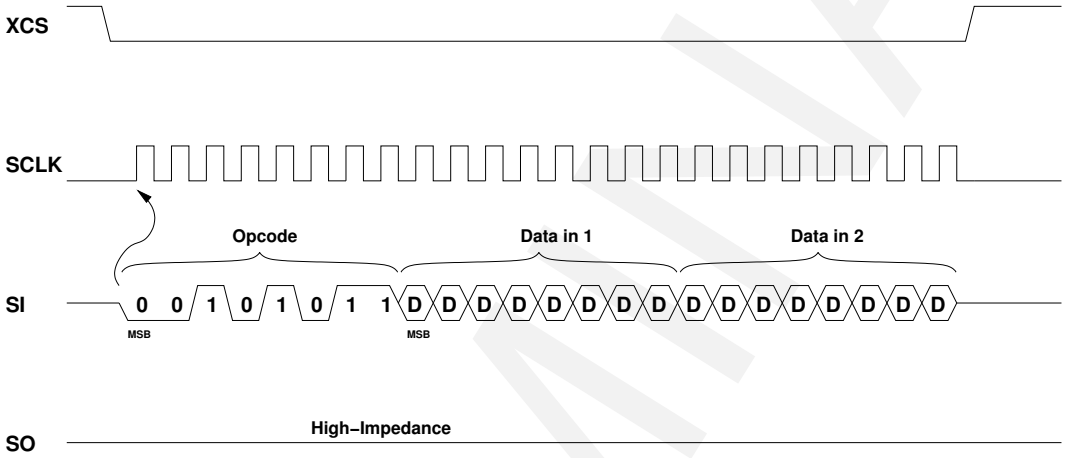


Figure 43: SPI Write Video Display Controller Control1

Video Display Controller Control1 register contains several parameters for Video Display Controller.

Bit	Name		Type	Description	
15	DIRDAC	Direct DAC Mode	W	0 1	Direct DAC disabled (default) Direct DAC enabled
14	TRUV	Translate U and V	W	0 1	U and V from SRAM (default) U and V from table
13	CLKSEL	Clock select	W	0 1	VXTAL as clock source (default) 8×PLL as clock
12	PLLENA	PLL enable	W	0 1	8×PLL and crystal oscillator are disabled (default) 8×PLL and crystal oscillator are enabled
11-3	DACDIV	Direct DAC clock divider bits 11-3	W	000h	High bits of divider (default)
2-0	UVSKIP	U and V skip cycles	W	0h > 0h	UV skip disabled (default) UV skip enabled

DIRDAC Bit DIRDAC bit controls The Direct DAC mode of the Video Display Controller. In default mode after power-up bit value is “0”, which means that Direct DAC mode is disabled.

Setting the bit “1” enables the Direct DAC mode and switches the controls of the Video Display Controller accordingly.

TRUV Bit TRUV bit controls the use of U and V translate table. In default mode after power-up bit value is “0” and U and V data comes directly from SRAM according to microcode program.

When bit is set to “1” the U and V translate is enabled. In that mode with the data from SRAM is selected one of four 4-bit values from U and V tables.

CLKSEL Bit CLKSEL bit selects the clock source of the Video Display Controller block. In default mode after power-up bit value is “0” and VXTAL crystal oscillator is used as clock input.

Setting the bit to “1” selects the output of 8x PLL as a clock source. Before the 8x PLL output can be selected as a clock source, 8x PLL has to be enabled by PLLENA bit and also it is good to check that the 8x PLL is locked to frequency of the VXTAL crystal oscillator.

PLLENA Bit PLLENA bit enables the 8x PLL and the crystal oscillator. In default mode after power-up bit value is “0” and PLL and crystal oscillator are in power-down state.

Setting the bit to “1” sets the 8x PLL and crystal oscillator on. Writing PLLENA bit high is also used for starting the 8x PLL lock check sequence. After the PLLENA write the lock status can be checked by a SPI read of Current Line Value & PLL Lock . If 8x PLL is locked, then it can be switched as clock source for Video Display Controller. However, if 8x PLL is not locked the 8x PLL lock check sequence can be started again by writing “1” to PLLENA bit.

The Video DAC uses signals (band gap reference voltage and current bias) which are generated by 8x PLL. If Video DAC output is used then the 8x PLL has to be enabled also beforehand.

DACDIV Bits These bits are the 9 MSBs of Direct DAC Mode clock divider. The 12-bit divider value is generated by concatenating DACDIV&”111” and the actual divider is DACDIV&”111”+1. The divider is used for dividing the Video Display Controller clock in Direct DAC mode so that lower frequency outputs can be generated. The divider range is from 8 to 4096 in increments of 8. The DACDIV default value is 000h.

UVSKIP Bits These three bits are used for skipping the U and V data fetching from the SRAM for the given amount of microcode program runs. In default mode after power-up value of the bits is “000” and no U and V command lines of microcode program are skipped.

By setting the bits to a value larger than “000” then in the amount of microcode program runs defined by the UVSKIP bits the U and V command lines are skipped. This can be used to allocate relatively more data space of SRAM to Y information when needed.

8.5 Write Picture Index Start Address (2Ch)

To write the Picture Index Start Address register XCS pin must be first asserted and opcode 2Ch clocked into the device. After that the two byte value is clocked in the device via SI pin. MSB is clocked in first. Bits 15 and 14 are zeroes. When XCS pin is deasserted the Picture Index Start Address register will be updated.

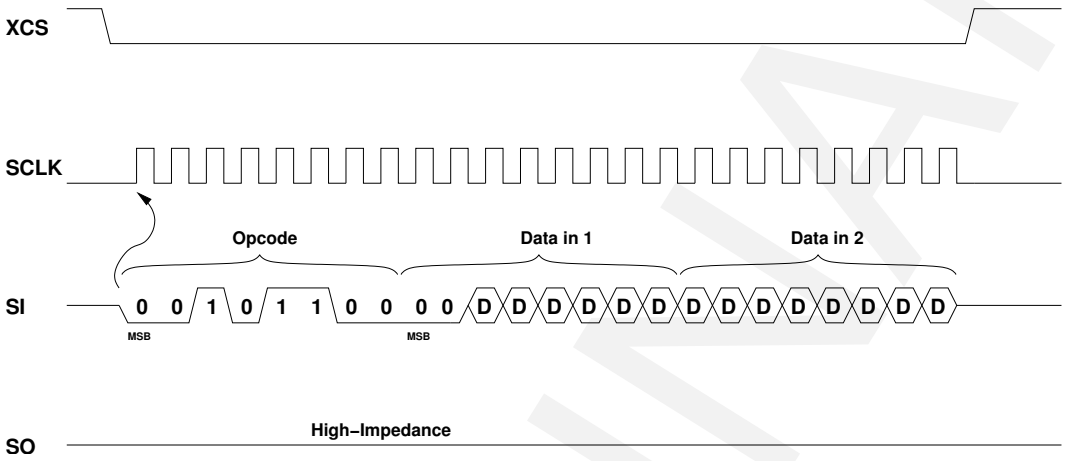


Figure 44: SPI Write Picture Index Start Address

The actual index start byte address is the register value shift left by two. At that address is the line index address of the line #0. Line index consists of three data bytes. Line index format is shown in detail in VS23S010D Guide. The line index addresses for consecutive lines are got by incrementing the picture index start byte address by three. The index addresses can be only in the first half of the SRAM.

If line index address is less than the index start byte address, then the current line is protoline, otherwise it is normal line (i.e. first protoline, then normal and finally end is again protoline). Note, that line index is a bit address and Picture Index Start Address has to be shift left by five for the above comparison.

Refer to VS23S010D Guide for more information about SRAM organization in Video Display Controller mode.

In Direct DAC mode the Index Start Address is used as the start address of DAC data buffer. The register value is shifted left by one to generate DAC data buffer start address, refer to VS23S010D Guide. In direct DAC mode all 16 bits of the Index Start address register are used. The value has to be larger than 0000h in Direct DAC mode.

8.6 Write Video Display Controller Control2 (2Dh)

To write the Video Display Controller Control2 register XCS pin must be first asserted and opcode 2Dh clocked into the device. After that two byte value is clocked in the device via SI

pin. The two byte value is input MSB (bit 15) first. When XCS pin is deasserted the Video Display Controller Control2 register will be updated.

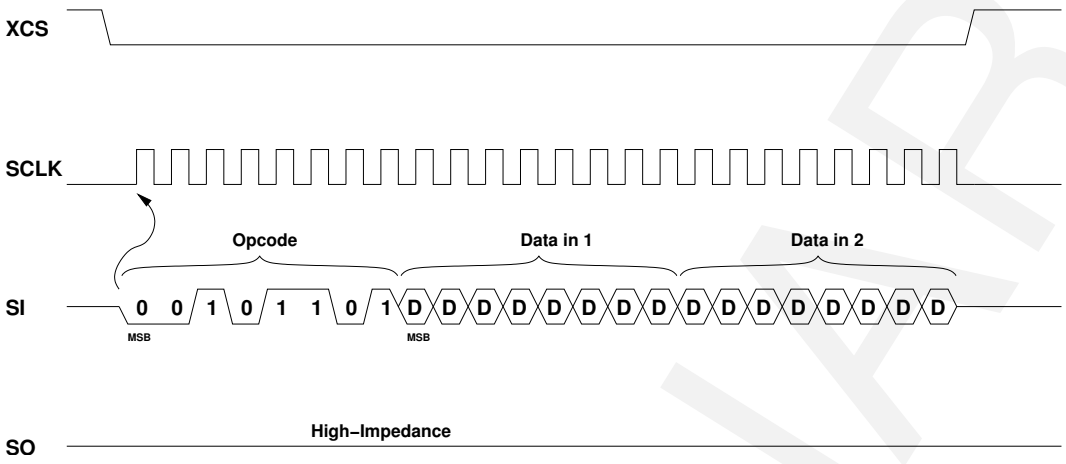


Figure 45: SPI Write Video Display Controller Control2

Video Display Controller Control2 register is written last to enable the Video Generator.

Video Display Controller Control2 register contains following parameters for Video Display Controller.

Bit	Name		Type	Description	
15	ENA	Enable Video Display Controller	W	0 1	Video Display Controller off (default) Video Display Controller on
14	VMOD	Video Mode	W	0 1	NTSC (default) PAL
13-10	PLEN	Program Length	W	0h >0h	PLEN+1 cycles, not allowed (default) PLEN+1 cycles, usable range
9-0	LCNT	Line Count	W	000h	LCNT+1 lines (default)

ENA Bit ENA bit enables the Video Display Controller. In default mode after power-up bit value is “0” and Video Display Controller is disabled.

Setting the bit to “1” will enable the Video Display Controller block. Before that the other Video Display Controller registers have to be written to correct values. Also line indexes and other video data need to be written to SRAM beforehand. It is of course possible to update video information in SRAM also when Video Display Controller is enabled.

VMOD Bit VMOD bit is used to select between NTSC and PAL mode video output. Default value is “0” which selects NTSC mode.

Setting bit high selects PAL mode. In that mode the phase of part of the color information on the video signal is reversed with each line, i.e. V signal is negated.

When NTSC mode is selected, the CSClk frequency is 3.579545 MHz. When PAL is selected, the CSClk frequency is 4.433618 MHz.

PLEN Bits PLEN bits define the amount of VClk cycles, which one run of the microcode program in normal line part lasts. The default value is 0h, which is not allowed. The protoline is not affected by these bits, there a program run lasts always eight cycles.

Write these bits to a value 1h or higher and then the program run lasts PLEN+1 VClk cycles.

LCNT Bits LCNT bits are used to define the line count of video picture. LCNT+1 is total amount of lines. Default value is 000h. Maximum amount of lines is 1024.

LCNT is used to define when the fetching of line indexes starts again from SRAM position given by Picture Index Start Address.

8.7 Write V Table (2Eh)

To write the V Table register XCS pin must be first asserted and opcode 2Eh clocked into the device. After that two byte value is clocked in the device via SI pin. The two byte value is input MSB (bit 15) first. When XCS pin is deasserted the V Table register will be updated.

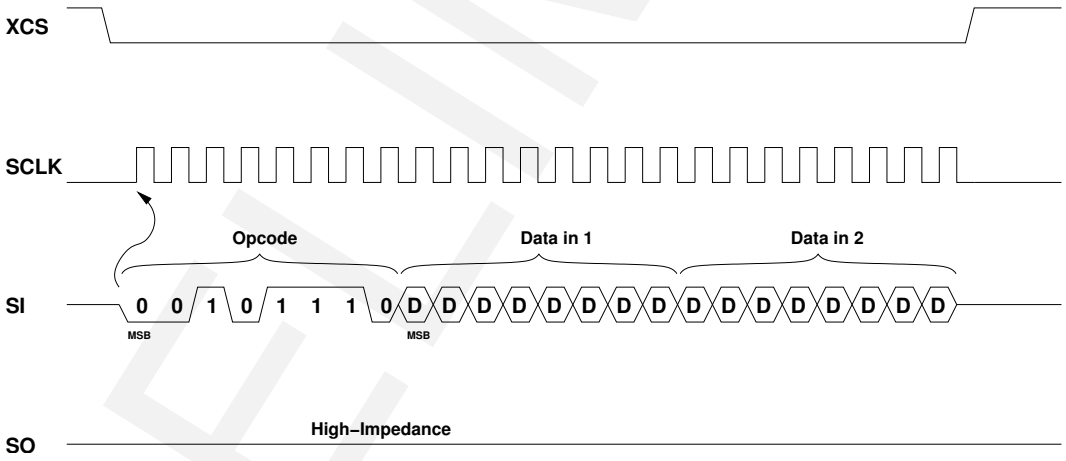


Figure 46: SPI Write V Table

Bit	Name		Type	Description	
15-12	V3	V Table Value #3	W	0h	V#3 (default)
11-8	V2	V Table Value #2	W	0h	V#2 (default)
7-4	V1	V Table Value #1	W	0h	V#1 (default)
3-0	V0	V Table Value #0	W	0h	V#0 (default)

V Table is a register where four four-bit V values can be set. Default value after power-up is 0000h. V Table is used when TRUV bit in Video Display Controller Control1 register is set to

high. The two V bits fetched from SRAM by the microcode program are used select one of four-bit values from register as V output to Color Modulator instead of the value from SRAM. With SRAM bits “00” V0 is select as output, “01” selects V1, “10” selects V2 and finally with “11” the output is V3.

With TRUV bit and this table it is possible to generate with two SRAM bits an V output that is not symmetrical to mid-value.

8.8 Write U Table (2Fh)

To write the U Table register XCS pin must be first asserted and opcode 2Fh clocked into the device. After that two byte value is clocked in the device via SI pin. The two byte value is input MSB (bit 15) first. When XCS pin is deasserted the U Table register will be updated.

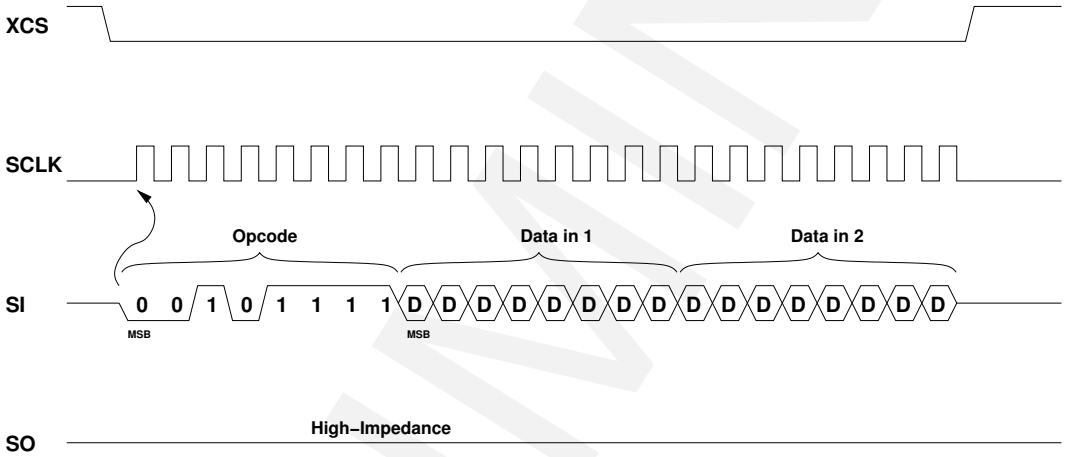


Figure 47: SPI Write U Table

Bit	Name		Type	Description	
15-12	U3	U Table Value #3	W	0h	U#3 (default)
11-8	U2	U Table Value #2	W	0h	U#2 (default)
7-4	U1	U Table Value #1	W	0h	U#1 (default)
3-0	U0	U Table Value #0	W	0h	U#0 (default)

U Table is a register where four four-bit U values can be set. Default value after power-up is 0000h. U Table is used when TRUV bit in Video Display Controller Control1 register is set to high. The two U bits fetched from SRAM by the microcode program are used select one of four-bit values from register as U output to Color Modulator instead of the value from SRAM. With SRAM bits “00” U0 is select as output, “01” selects U1, “10” selects U2 and finally with “11” the output is U3.

With TRUV bit and this table it is possible to generate with two SRAM bits an U output that is not symmetrical to mid-value.

8.9 Write Program (30h)

To write the Program register XCS pin must be first asserted and opcode 30h clocked into the device. After that four byte value is clocked in the device via SI pin. The four byte value is input MSB (bit 31) first. When XCS pin is deasserted the Program register will be updated.

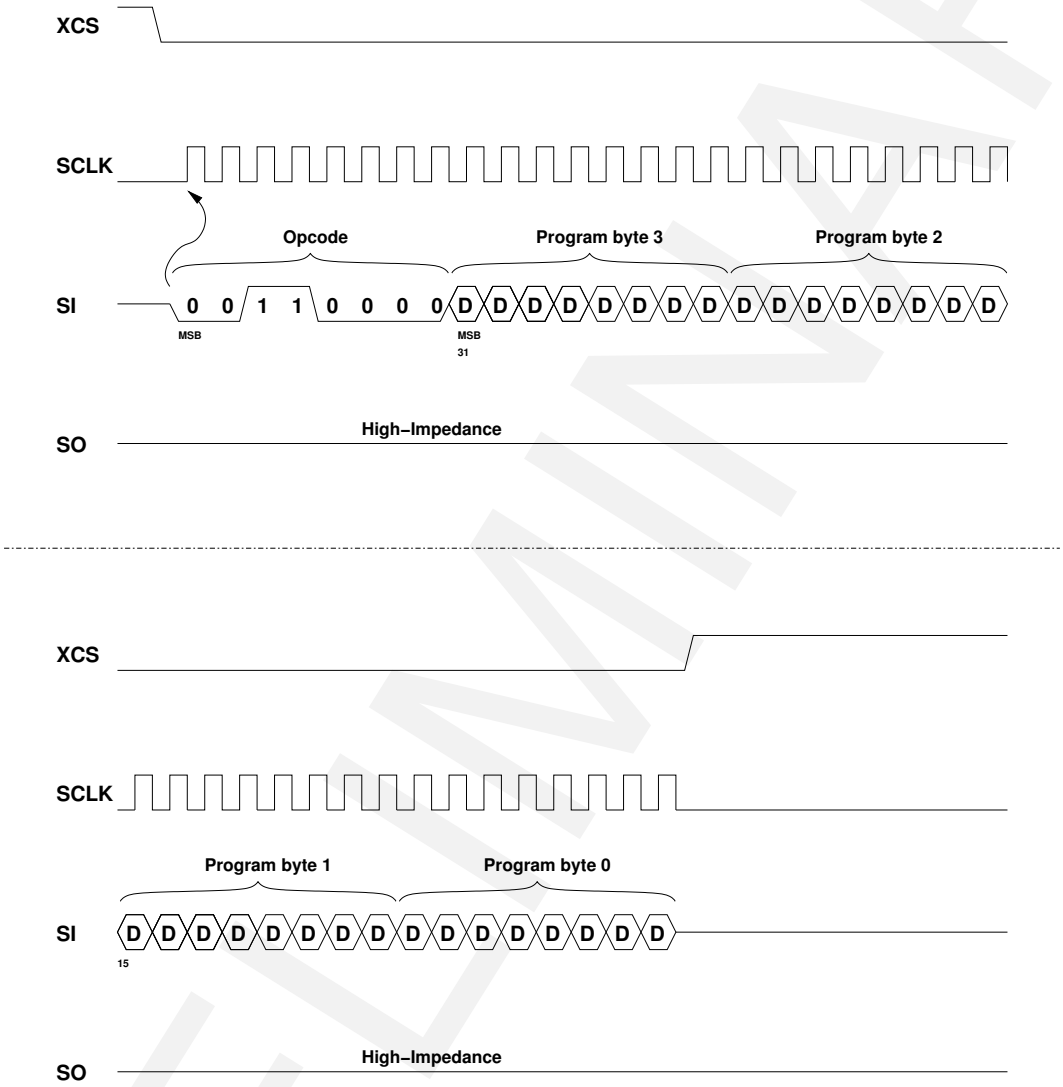


Figure 48: SPI Write Program

The Program register contains four lines (bytes) of microcode for the Video Generator. The next table shows the coding for one command line (byte). All four program bytes have the same coding. The default value of Program is 0000h after power-up.

Bit	Name		Description	
7-6	CC	Command Code	00 01 10 11	Pick a (V) (default) Pick b (U) Pick y (Y) Pick -
5-3	BA	Bit Amount	000	Amount of bits taken (range 1 to 8) (default)
2-0	DS	Data Shifts	000	Amount of data shifting (range 0 to 6) (default)

CC Bits CC Bits are the command code for the operation. Pick a takes the V value either straight from SRAM data or from the V Table. Pick b takes the U value either straight from SRAM data or from the U Table. Pick y takes the Y value from the SRAM data. Pick - does not take any value, but it may do data shifting.

BA Bits The amount of bits taken is BA+1. For U and V there is an upper limit of six bits. If U and V tables are used then two bits are needed for U and V.

DS Bits DS bits define the shift amount of data. The shifts should equal the amount of bits taken. The shift range is from 0 to 6. If more than six bits are taken, then the rest of the shifts should be done on the next program cycle.

The program below translates to following 32-bit word, C4BC5C1Ch. Cycle 0 is in bits 7-0, cycle 1 in bits 15-8 and so on.

```
                pick            bits        shift
cycle           a|b|y|-         1...8       0...6

0               a               4           4       // take V(4), shift 4
1               b               4           4       // take U(4), shift 4
2               y               8           4       // take Y(8), shift 4
3               -               x           4       // idle, shift 4
```

Note, that the program defines the order of video data in SRAM. The data order in SRAM is the same as the order and amount of data taken in the microcode program.

8.10 Read Current Line and PLL Lock (53h)

The 10-bit Line Counter value can be read to determine on what line of the video picture the Video Display Controller is at the end of the SPI command. Additionally, 8x PLL lock state is given as is the state of the Video Generator Block Move, which is also shown on MVBLK pin.

To read the Video Display Controller Frame Length register XCS pin must be first asserted and opcode 53h clocked into the device. After that two byte value is clocked out from the device via SO pin. The two byte value is output MSB (bit 15) first. When XCS pin is deasserted, the clocking out of data is ended and SO pin goes to high-impedance state.

Bit	Name		Type	Description	
15	PLLLCK	8×PLL Lock	R	0 1	PLL not locked (default) PLL locked
14	MVBS	Block Move State	R	0 1	Block move idle (default) Block move active
9-0	CL	Current Line	R	000h	Line counter value (default)

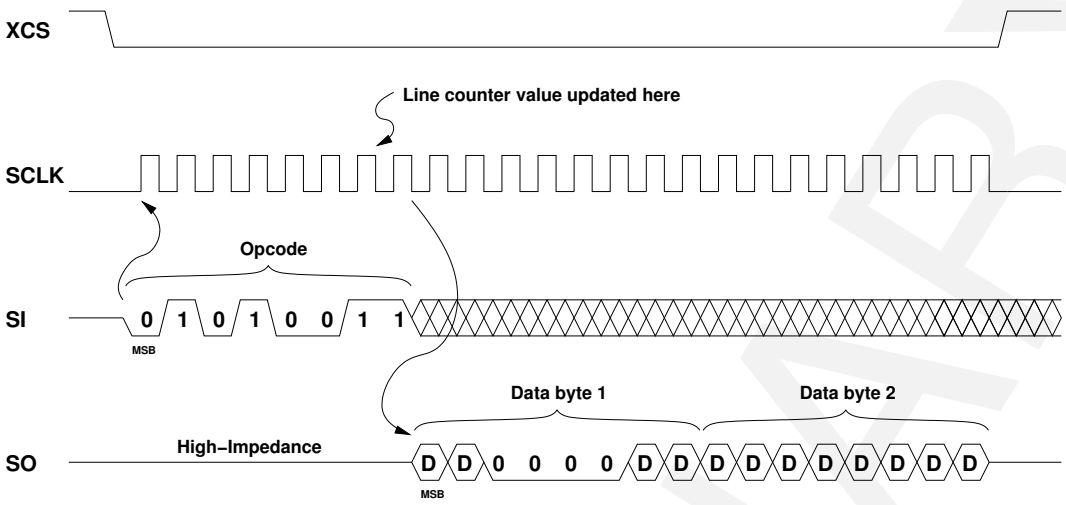


Figure 49: SPI Read Current Line and PLL Lock

PLLLCK Bit PLLLCK is used to signal if the 8x PLL is locked to incoming VXTAL crystal oscillator frequency. The default value after power-up is “0” and 8x PLL is not locked when low value is read. If bit is high, 8x PLL is locked.

The PLL lock check sequence is described in Chapter 8.4.

MVBS Bit The default value of MVBS is “0” and block move is inactive then. If bit is high, then block move is under way.

CL Bits These bits show the current value of the Video Display Controller Line counter. Default value after reset is 000h. The range is from 0 to 1023. When the value is read, it is updated just before the SPI command is received by the VS23S040D.

8.11 Write Block Move Control1 (34h)

To write the Block Move Control1 register XCS pin must be first asserted and opcode 34h clocked into the device. After that five byte value is clocked in the device via SI pin. The five byte value is input MSB (bit 39) first. When XCS pin is deasserted the Block Move Control1 register will be updated.

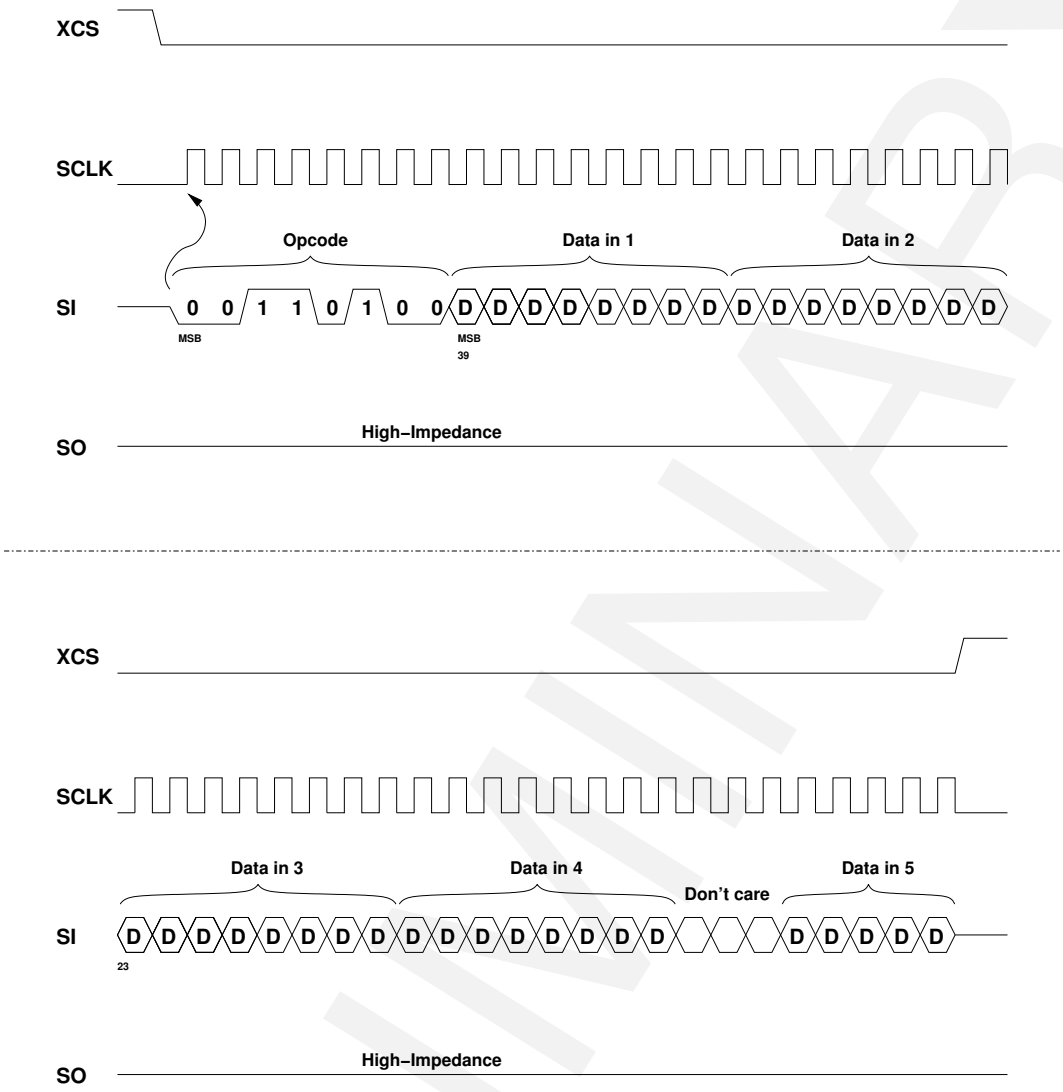


Figure 50: SPI Write Block Move Control1

Bit	Name		Type	Description	
39-24	MVSRC	Source Address	W	0000h	Source address bits 16-1 (default)
23-8	MVTGT	Target Address	W	0000h	Target address bits 16-1 (default)
4	PYF	Low-pass Y Filter	W	0 1	Filter disabled (default) Filter enabled
3	DACC	DAC Control	W	0 1	Large current mode (default) Small current mode
2	MVSRC0	Source Address	W	0	Source address bit 0 (default)
1	MVTGT0	Target Address	W	0	Target address bit 0 (default)
0	MVDIR	Move Direction	W	0	Move forward (default) Move backward

Block Move is described generally in VS23S010D Guide.

MVSRC, MVSRC0 Bits MVSRC bits define the 17-bit wide byte source start address for block move. The default value is 00000h. The address points to the first byte of the block. Note, address bit 0 is in position 2 of the 40-bit wide control word.

MVTGT, MVTGT0 Bits MVTGT bits define the 17-bit wide byte target address for block move. The default value is 00000h. The address points to the first byte of the block target area. Note, address bit 0 is in position 1 of the 40-bit wide control word.

PYF Bit PYF bit is used to enable the low-pass luminance filter. The default value after reset is “0” and the filter is disabled. To enable the filter write “1” to PYF bit.

DACC Bit DACC bit is used to control Video DAC current. The default value set in reset is “0” which puts the Video DAC to large current mode. To change the Video DAC to small current mode write DACC bit to “1”. Small current mode can be used with an external op amp.

MVDIR Bit This bit selects the block move direction. The default value after reset is “0” and so the move direction is forward (i.e. SRAM addresses increase). By setting the bit high the move direction changes to backward (i.e. SRAM addresses decrease).

Note, when MVDIR bit is high, the MVSRC address is the for the last byte to be moved and also the MVTGT address is for the last target byte position.

8.12 Write Block Move Control2 (35h)

To write the Block Move Control2 register XCS pin must be first asserted and opcode 35h clocked into the device. After that four byte value is clocked in the device via SI pin. The four byte value is input MSB (bit 31) first. The five MSBs of the data are don’t cares. When XCS pin is deasserted the Block Move Control2 register will be updated.

Bit	Name		Type	Description	
26-16	MVSKP	Block Move Skip	W	000h	Skip between lines (default)
15-8	MVLEN	Block Move Length	W	00h	Length of block (X dir.) (default)
7-0	MVLIN	Block Move Lines	W	00h	Amount of lines (Y dir.) (default)

MVSKP Bits MVSKP bits define the amount of bytes between two lines of the moved block. The default value is 000h and the range is from 1 to 2048 (i.e. the actual amount of bytes is MVSKP+1).

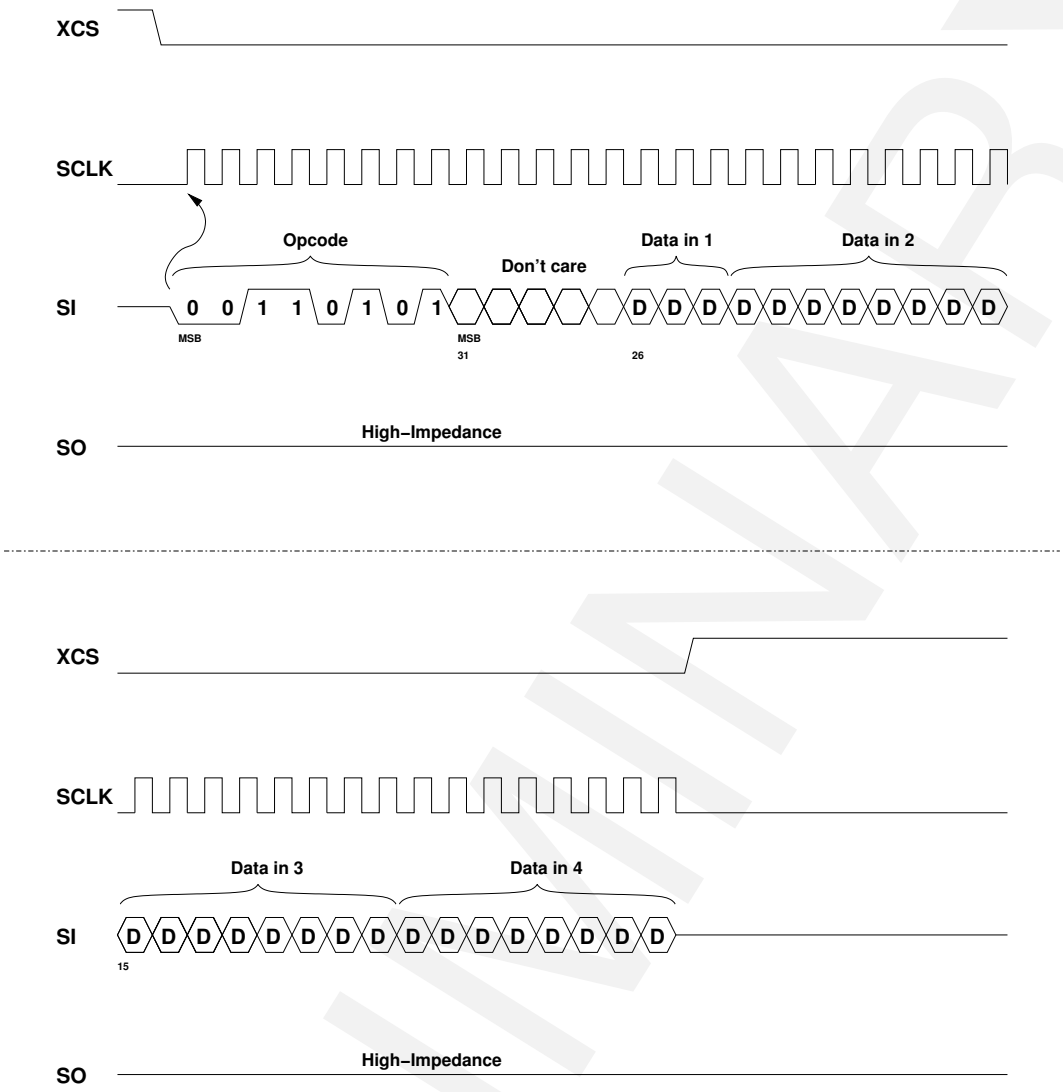


Figure 51: SPI Write Block Move Control2

MVLEN Bits The MVLEN bits are used to define how many consecutive bytes belong to the block to be moved. The MVLEN bits can be described as the X dimension of the block. The default value after power-up is 00h and the range varies from 0 to 255.

MVLIN Bits The MVLIN bits are used to define how many lines belong to the block to be moved. The MVLIN bits can be described as the Y dimension of the block. The default value after power-up is 00h and the range varies from 1 to 256 (i.e. the actual amount of lines is MVLIN+1).

8.13 Start Block Move (36h)

Start Block Move command is a one-byte command used to enable a single block move operation. Before writing this command set the Block Move Control registers to correct values.

Check also that the previous block move is already finalized, i.e. MVBLK pin is low or MVBS bit is low, when Video Display Controller Status register is read.

To write the Start Block Move register XCS pin must be first asserted and opcode 36h clocked into the device. When last bit of opcode is received the Block Move operation begins. After writing the byte XCS pin is deasserted.

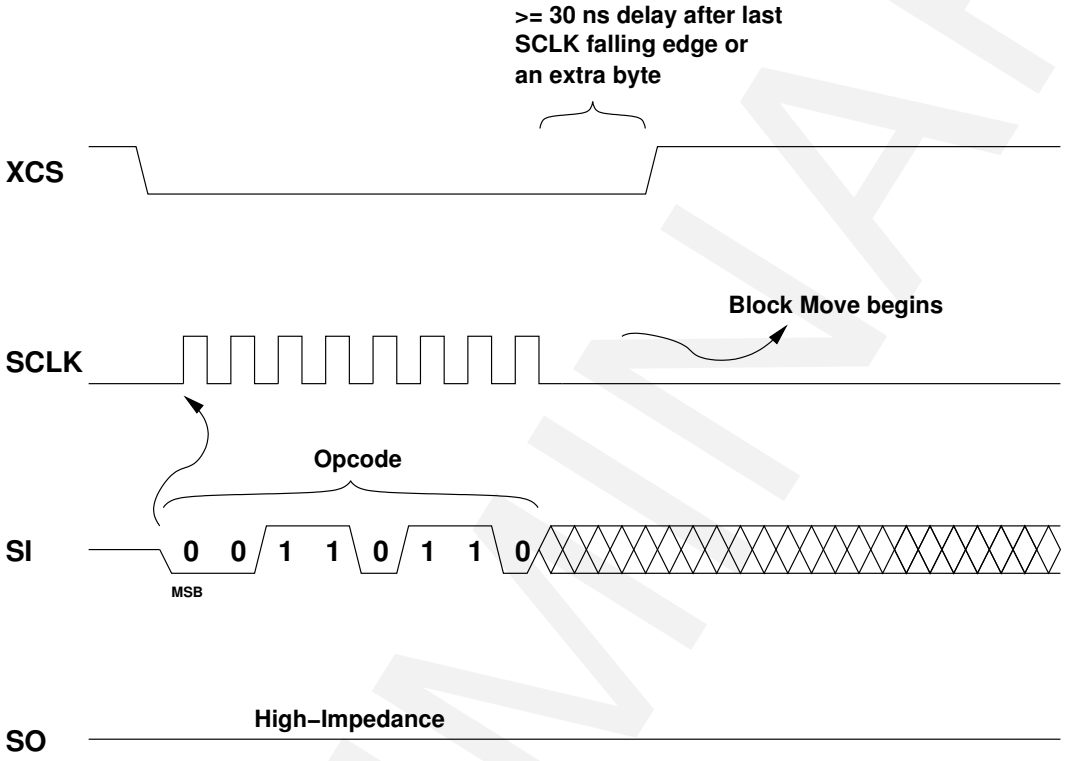


Figure 52: SPI Write Block Move Start

9 8-Bit Parallel Interface Commands and Addressing

8-bit parallel interface is an 8080 and NAND Flash type interface. It is an alternative interface to SRAM and when it is used the SPI interface must be inactive. So, XCS pin must be set high when 8-bit parallel interface is used.

A valid 8-bit interface operation is started by first asserting XCSPAR pin. After that the host controller clocks out a valid 8-bit opcode. Following the opcode are three address bytes sent by the host controller. If there is a write operation the host sends data bytes to the device. In read operation the device starts clocking out data one clock cycle after the address. The operation is ended by deasserting the XCSPAR pin.

9.1 8-Bit Parallel Interface Read

The Read command can be used to sequentially read a continuous stream data from the device by providing clock signal once the initial starting address has been specified. The device has on internal address counter that increments on every cycle.

To perform a read operation, XCSPAR must first be asserted and read opcode 03h must be clocked into device. After the opcode three address bytes are clocked into the device to specify the starting address location of the first byte to read within SRAM. Note, that two LSBs of the address have to be zeros always.

After address bytes additional clock cycles will result in data being output on the parallel interface. When the last byte (7FFFFh) of the SRAM has been read, the reading will continue from the beginning of the array (00000h).

Deasserting the XCSPAR pin will terminate the read operation and parallel interface goes to high-impedance state.

9.2 8-Bit Parallel Interface Write

Prior to writing the device must be selected by bringing XCSPAR pin low. Once the device is selected the Write command can be started by issuing a Write instruction (opcode 02h) followed by a 24-bit address. Note, that two LSBs of the address have to be zeros always.

The device works in sequential mode where after the initial data byte additional bytes can be clocked into device. The internal address pointer is automatically incremented. When the internal address pointer reaches its maximum value (7FFFFh) it rolls over to 00000h. This allows the operation to continue indefinitely, however, previous data will be overwritten. Note, that the amount of written data bytes has to be a multiple of four, e.g. 4, 8, 12, 16 and so on. Also note that after last byte at least one dummy byte is needed by the VS23S040D.

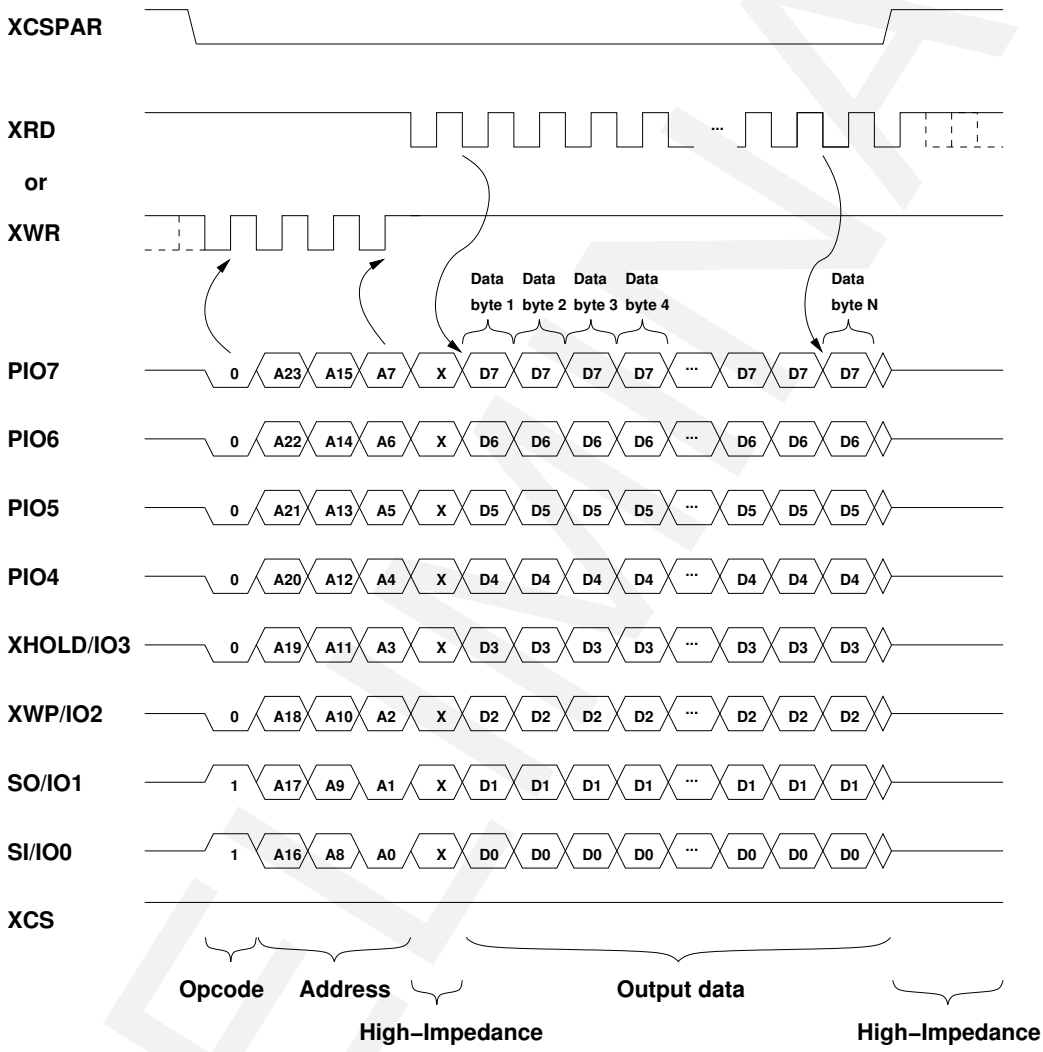


Figure 53: 8-Bit Parallel Interface Read

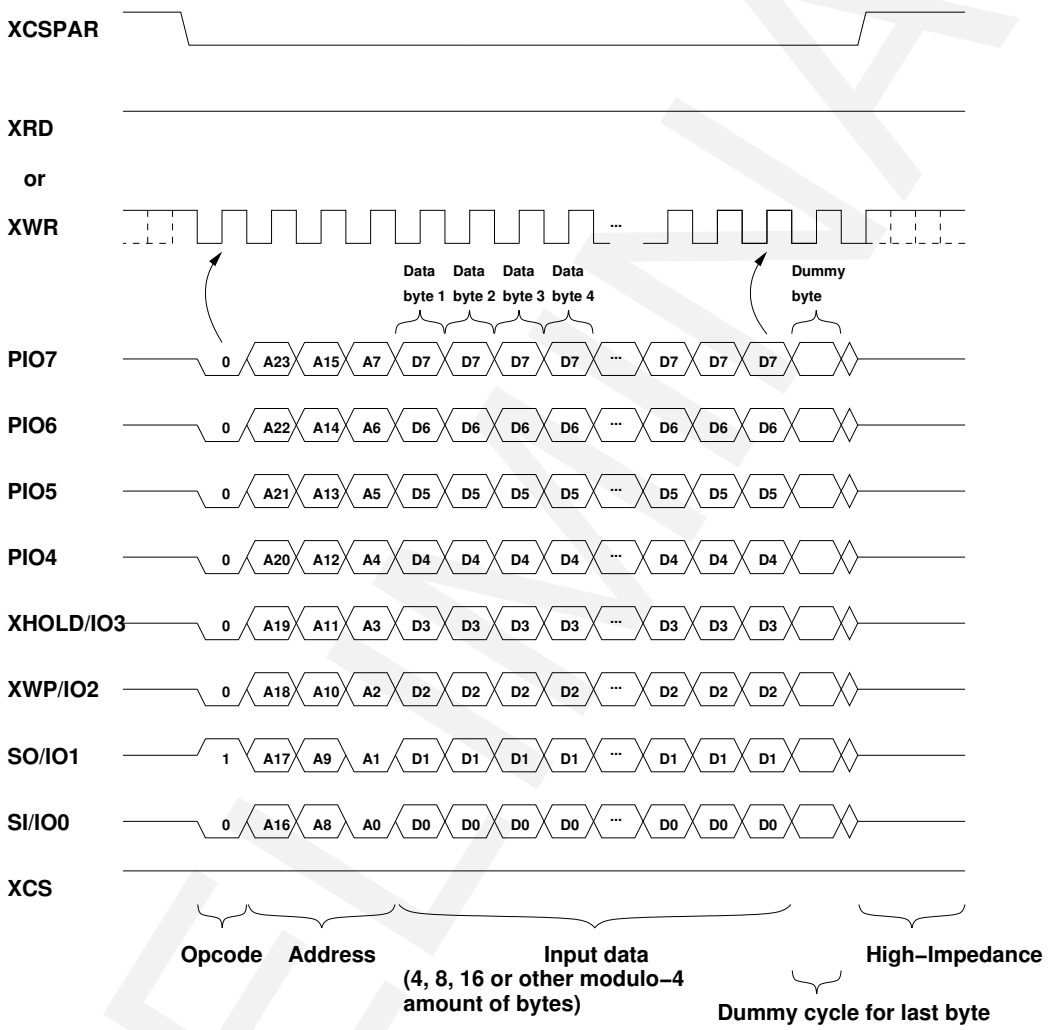


Figure 54: 8-Bit Parallel Interface Write

10 Document Version Changes

This chapter describes the most important changes to this document.

Version 0.4, 2018-10-01

- Updated Chapter 3

Version 0.3, 2017-12-12

- Changed couple of words to bytes.
- Fixed Chapter 6.1.4
- Added web address of BGA24 package dimension drawing.

Version 0.2, 2017-11-10

- Updated section 3
- Added Video&Registers Block notion for specified logic blocks

Version 0.1, 2017-07-05

- Initial version based on VS23S010D datasheet

11 Contact Information

VLSI Solution Oy
Entrance G, 2nd floor
Hermiankatu 8
FI-33720 Tampere
FINLAND

URL: http://www.vlsi.fi/
Phone: +358-50-462-3200
Commercial e-mail: sales@vlsi.fi

For technical support or suggestions regarding this document, please participate at
http://www.vsdsp-forum.com/
For confidential technical discussions, contact
support@vlsi.fi