VS1011 to VS1003 Migration Guide

Description

This document describes how to migrate from VS1011 to VS1003. It lists hardware and software differencies and other considerations.

This document applies to all versions of VS1011 and VS1003.

Revision History			
Rev	**Date**	**Author**	**Description**
1.13	2025-04-03	HH	Corrected version number / history.
1.12	2023-12-22	POj	Clarifications for CLOCKF and CVDD.
1.11	2019-02-04	POj	Contact information updated.
1.01	2012-11-28	HH	Minor updates.
1.00	2012-11-21	HH	Initial revision.

Contents

1 General

VS1003 has many updated features compared to VS1011. The most significant differences are:

- VS1011 and VS1003 have different operating voltages,
  VS1003 has an additional supply voltage pin CVDD.
- VS1003 is not available in the SOIC-28 package.
- VS1003 doesn't have optional MP1 and MP2 decoding. If you need these, see vs1053b instead.
- VS1003 has a mono analog differential microphone / one-sided line input.
- VS1003 can encode the analog input into IMA ADPCM.
- VS1003 can decode WMA.
- VS1003 can decode and play General MIDI files with an internal synthesizer.
- VS1003 has a UART so it can be connected to VSIDE.
- VS1003 has an internal PLL and a control register for it.

Due to these new features the pin-out and register interface has been changed accordingly.

1.1 Checklist with Recommendations

- Use the LQFP-48 package.
- Add a separate voltage regulator for CVDD.
- Use vs1053b/vs1063a pinout for the board to be forwards-compatible.
- Use 12.288 MHz crystal, check what your software writes to SCI_CLOCKF.
- If your code loads user code/patches to vs1011, remove those. Check if you need the corresponding ones for the replacement.
- If you don't want to play some formats, monitor the contents of HDAT registers and stop playing if you see forbidden formats.

2 Hardware

VS1011 and VS1003 have a few hardware differences.

2.1 New: Core Voltage, Changed: Analog Voltage

The biggest difference is the addition of Core Voltage in VS1003. In addition to Analog and Digital (IO) Voltage the VS1003 features a separate voltage input for the VSDSP core. This voltage can be in the range of 2.4 V. . . 2.85 V.

With VS1011 the analog voltage AVDD could be 2.5 V. . . 3.6 V. The VS1003 range for AVDD is 2.6 V. . . 2.85 V.

With VS1011 it was easy to implement a system where only one operating voltage, between 2.5 and 3.6 V, was used. In year 2011 VS1003 was requalified to also allow operation on a single voltage. The common area for the three voltages is 2.6 V. . . 2.85 V.

Note: some SD cards require a voltage of at least 2.8 V, which may limit the usable voltage area in real systems using SD cards.

While you might be able use a single voltage supply, it is highly recommended to use a separate regulator for CVDD to be forwards-compatible with newer chips such as vs1053b and vs1063a. You don't need board changes to populate a different CVDD regulator and decoder. See vs1053b / vs1063a datasheets for pinouts.

2.2 New: Internal PLL

VS1003 has an internal PLL that can be used to generate an internal clock sufficiently high for WMA and MIDI decoding. See more info on the PLL and the associated SCI_CLOCKF register in the *VS1003 Datasheet*.

VS1003 has a VCO output pin. This pin is used for testing only and should be left unconnected.

2.3 Changed: Clocking

If you used 12.288 MHz crystal and clock doubler with vs1011, you may not need any changes to clocking or SCI_CLOCKF.

VS1011 is clocked with either a 24. . . 26 MHz or 12. . . 13 MHz crystal. In the latter case an internal clock doubler of vs1011 can be used to achieve internal clock speed of up to 26 MHz.

VS1003 is clocked with a 12. . . 13 MHz clock. Then the PLL of VS1003 is used to increase the internal clock to speeds up to 52 MHz. The suggested crystal for VS1003 is 12.288 MHz.

2.4 New: Differential Microphone / One-Sided Line Input

VS1003 features a differential microphone and one-sided line-level input. One of these inputs can be used to record ADPCM audio. The SCI_MODE register can be used to select the input.

2.5 Changed: LQFP-48 and BGA-49 Pin Descriptions

The following table describes the new pins and functions for VS1003.

See dimensions for LQFP and BGA (depreciated) packages from *http://www.vlsi.fi/* .

Both LPQFP-48 and BGA-49 are lead (Pb) free and also RoHS compliant packages. RoHS is a short name of *Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment*.

Pin descriptions:

Pin Name	LQFP-48 Pin	BGA49 Ball	Pin Type	New Function for VS1003
MICP	1	C3	AI	Microphone input, new for VS1003.
MICN	2	C2	AI	Microphone input, new for VS1003.
XRESET	3	B1	DI	
DGND0	4	D2	DGND	
CVDD0	5	C1	CPWR	Core power, new for VS1003.
IOVDD0	6	D3	IOPWR	Only I/O Power in VS1003.
CVDD1	7	D1	CPWR	Core power, new for VS1003.
DREQ	8	E2	DO	
GPIO2 / DCLK	9	E1	DIO	
GPIO3 / SDATA	10	F2	DIO	
XDCS / BSYNC	13	E3	DI	
IOVDD1	14	F3	IOPWR	Only I/O Power in VS1003.
VCO	15	G2	DO	For testing purposes (don't connect), new for VS1003
DGND1	16	F4	DGND	
XTALO	17	G3	AO	
XTALI	18	E4	AI	
IOVDD2	19	G4	IOPWR	Only I/O Power in VS1003.
IOVDD3		F5	IOPWR	I/O Power in VS1003, DGND4 digital ground in VS1011! (Note: This major difference only in BGA package)
DGND2	20		DGND	
DGND3	21	G5	DGND	
DGND4	22	F6	DGND	
XCS	23	G6	DI	
CVDD2	24	G7	CPWR	Core power, new for VS1003.
RX	26	E6	DI	UART receive, new for VS1003.
TX	27	F7	DO	UART transmit, new for VS1003.
SCLK	28	D6	DI	
SI	29	E7	DI	
SO	30	D5	DO3	
CVDD3	31	D7	CPWR	Core power, new for VS1003.
TEST	32	C6	DI	Connect to IOVDD instead of VDD on VS1003.
GPIO0 / SPIBOOT	33	C7	DIO	Use 100 kΩ pull-down resistor if you don't want SPI Boot
GPIO1	34	B6	DIO	
AGND0	37	C5	APWR	
AVDD0	38	B5	APWR	
RIGHT	39	A6	AO	
AGND1	40	B4	APWR	
AGND2	41	A5	APWR	
GBUF	42	C4	AO	
AVDD1	43	A4	APWR	
RCAP	44	B3	AIO	
AVDD2	45	A3	APWR	
LEFT	46	B2	AO	
AGND3	47	A2	APWR	
LINEIN	48	A1	AI	Line input, new for VS1003.

Pin types:

Type	Description
DI	Digital input, CMOS Input Pad
DO	Digital output, CMOS Input Pad
DIO	Digital input/output
DO3	Digital output, CMOS Tri-stated Output Pad
AI	Analog input

Type	Description
AO	Analog output
AIO	Analog input/output
APWR	Analog power supply pin
DGND	Core or I/O ground pin
CPWR	Core power supply pin
IOPWR	I/O power supply pin

3 Application Considerations

This chapter gives general info on applications using VS1003.

3.1 Hardware Design

PCB traces from analog connections (particularly mic and line inputs) should be kept as short as possible.

Each voltage input pin should be bypassed with 100 nF capacitor for best performance.

Ground plane should be used under the VS1003. Each ground pin should be connected to this plane as close to the chip as possible.

3.2 Software Considerations

Fast Forward and Rewind operations differ between different audio formats. MP3 and WAV are well suited for random access and can be fast forwarded and rewinded as with VS1011. WMA and Midi need special attention.

If you don't want the product to play WMA and/or MIDI, you can use SCI_HDAT1 register to determine the currently playing file type. You can then skip the file if the format is something you don't want played. See the *VS1003 Datasheet* for detailed info.

4 SCI Registers

VS1011 and VS1003 have a few differencies in registers that are not compatible with each other. Extreme care should be taken when porting VS1011 microcontroller software to VS1003. The following chapters list some of these differencies. For more info on the registers, see *VS1011 Datasheet* and *VS1003 Datasheet*.

4.1 Changed: SCI_MODE

SM_LAYER12 changed to SM_SETTOZERO because VS1003 doesn't have MP1 or MP2 decoding.

SM_PDOWN, a "powerdown lite" mode was added to VS1003.

SM_ADPCM, SM_ADPCM_HP and SM_LINEIN added to control audio recording in ADPCM format.

4.2 Changed: SCI_STATUS

SS_VER is 1 for VS1011B, 2 for VS1011E, and 3 for VS1003.

4.3 Changed: SCI_CLOCKF

If you used 12.288 MHz crystal and clock doubler with vs1011, you may not need any changes.

In vs1011 SCI_CLOCKF is used to tell if the input crystal is something else than 24.576 MHz, and to activate its optional clock doubler.

VS1003 has an internal PLL which can be run at 0.5×XTALI steps between 1.0× and 6.0× (but without exceeding the maximum internal clock CLKI = 52.0 MHz). This PLL is controlled with the same register SCI_CLOCKF.

The suggested crystal for vs1003 is 12.288 MHz. With vs1003 a good default for SCI_CLOCKF is 0x8000 (for 3.0× clock), which is the same value that vs1011 uses with a 12.288 MHz crystal and clock doubler activated.

Read the *VS1003 Datasheet* for more details.

4.4 Changed: SCI_HDAT0 and SCI_HDAT1

These registers give info on the supported audio formats. With the new codecs supported in VS1003 these registers contain new info.

5 User Applications

Because the memory addresses have changed the user applications, plugins and patches are different between VS1011 and VS1003.

6 Microcontroller Examples

Examples on how to control VS1003 using a microcontroller are available at *http://www.vlsi.fi/en/support/software/microcontrollersoftware.html*

7 Latest Document Version Changes

This chapter describes the most important changes to this document.

Version 1.13, 2025-04-03

- Recommendation to use separate CVDD regulator for forwards-compatibility.
- Other recommendations in a checklist format.
- Corrected version numbering.

Version 1.12, 2023-12-22

- Some clarifications to information about CLOCKF and CVDD.

Version 1.11, 2019-02-04

- Contact information updated.

Version 1.01, 2012-11-28

- Added Chapter 6, *Microcontroller Examples*.
- Added mention of different AVDD's to Chapter 2.1.

8 Contact Information

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