VS10XX AppNote: I2S DAC

Description

This document describes how to interface VS10XX to an I2S DAC. It shows an example schematic and shows the required register settings.

This document applies to VS1033.

For detailed info on VS10XX registers see datasheets at http://www.vlsi.fi/datasheets/

Revision History			
Rev	**Date**	**Author**	**Description**
1.00	2006-01-04	PLe	Initial revision.
1.01	2006-06-12	PLe	Updated to VS1033.

Table of Contents

List of Figures

1 General Info on VS10XX I2S Interface

VS1033 has an I2S output that can be used to interface an external DAC. The inteface supports sample rates of 48 kHz, 96 kHz and 192 kHz. In I2S mode the GPIO pins are used as I2S output pins.

The word length of the interface is 16 bits per channel and a total of 32 bits per frame.

The GPIO pins in I2S mode		
Pin	**Function**	**Signal**
GPIO0	I2S bit clock	I2S_SCLK
GPIO1	I2S data output	I2S_DATA
GPIO4	I2S sample clock (the left/right output)	I2S_LROUT
GPIO5	I2S master clock	I2S_MCLK

Note: Other GPIO pins (GPIO2, GPIO3, GPIO6 and GPIO7) can be used as normal GPIO pins. If they are not used they should be conneted to ground with a 100k pull-down resistor.

2 Setting Up the I2S Interface

After hardware reset the I2S interface is disabled and all GPIO pins are set as inputs.

2.1 Setting Up IO Pins

The GPIO pins must be initialized to outputs before activating the I2S interface. To do this write 0xC017 to register SCI_WRAMADDR and 0x33 to SCI_WRAM.

2.2 Setting Up I2S Configuration Register

The I2S interface is set up by writing appropriate values to I2S_CONFIG register.

I2S configuration register				
Reg	**Type**	**Reset**	**Abbrev**	**Description**
0xC040	r/w	0	I2S_CONFIG[3:0]	I2S configuration

I2S_CONFIG Bits		
Name	**Bits**	**Description**
I2S_CF_MCLK_ENA	3	Enables the MCLK output (12.288 MHz)
I2S_CF_ENA	2	Enables I2S, otherwise pins are GPIO
I2S_CF_SRATE	1:0	I2S rate, "10" = 192, "01" = 96, "00" = 48 kHz

I2S is enabled by setting the I2S configuration register (0xC040) bit I2S_CF_ENA bit.

The I2S_CF_MCLK_ENA bit enables the MCLK output. The frequency is either directly the input clock (nominal 12.288 MHz), or half the input clock when mode register bit SM_CLK_ RANGE is set to 1 (24. . . 26 MHz input clock).

I2S_CF_ SRATE controls the output samplerate. When set to 48 kHz, SCLK is MCLK divided by 8, when set to 96 kHz SCLK is MCLK divided by 4, and when set to 192 kHz SCLK is MCLK divided by 2.

For example: to enable the I2S interface with MCLK enabled and 48kHz sample rate write 0xC040 to SCI_WRAMADDR and 0x0C to SCI_WRAM.

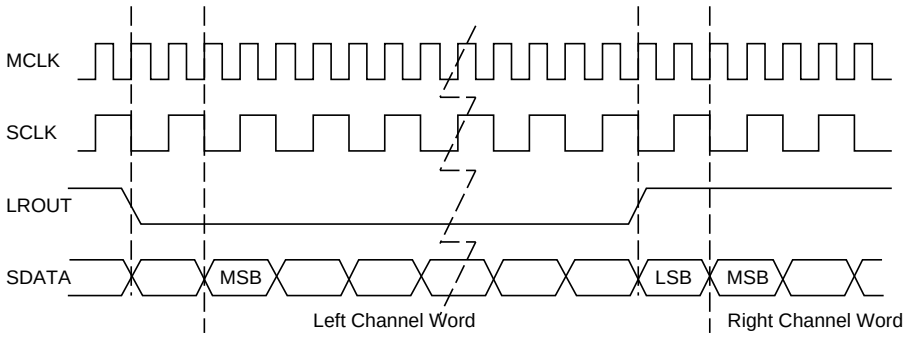

Figure 1: I2S Interface, 192 kHz.

I2S DAC's often support a variety of sample rates. Usually they work correctly with pretty much any sample rate as long as the different clock signals are in correct ratio with each other. VS10XX converts all audio it decodes to correct rate so that it plays at correct speed regardless of the sample rate of the original file. If MCLK output of VS10XX is used the DAC will stay in sync and convert the audio correctly. However, if for example 44.1kHz output sampling rate is reguired it can be achieved by using a 11.2896MHz crystal and by setting SM_CLK_RANGE to zero.

After I2S interface is set up the chip can be used normally. The decoded audio data is sent to I2S pins.

2.3 Example Code

The following pseudo code shows how to set up I2S after hardware reset. Also remember to set up other relevant VS10XX registers.

```
10 /* Set GPIO as outputs */
20 WriteRegister(SCI_WRAMADDR, 0xC017)
30 WriteRegister(SCI_WRAM, 0x0033)
40 /* Enable I2S (MCLK enabled, 48kHz sample rate)*/
50 WriteRegister(SCI_WRAMADDR, 0xC040)
60 WriteRegister(SCI_WRAM, 0x000c)
```

3 Example Schematic

Figure 2 shows a way to connect an I2S DAC to VS1033. Only the I2S related connections are shown.

Notice that the DAC's clock input (SCKI) is connected to I2S_MCLK of VS1033. This way the DAC and VS1033 stay in proper sync. GPIO0 pin has been pulled to ground to prevent SPI boot.

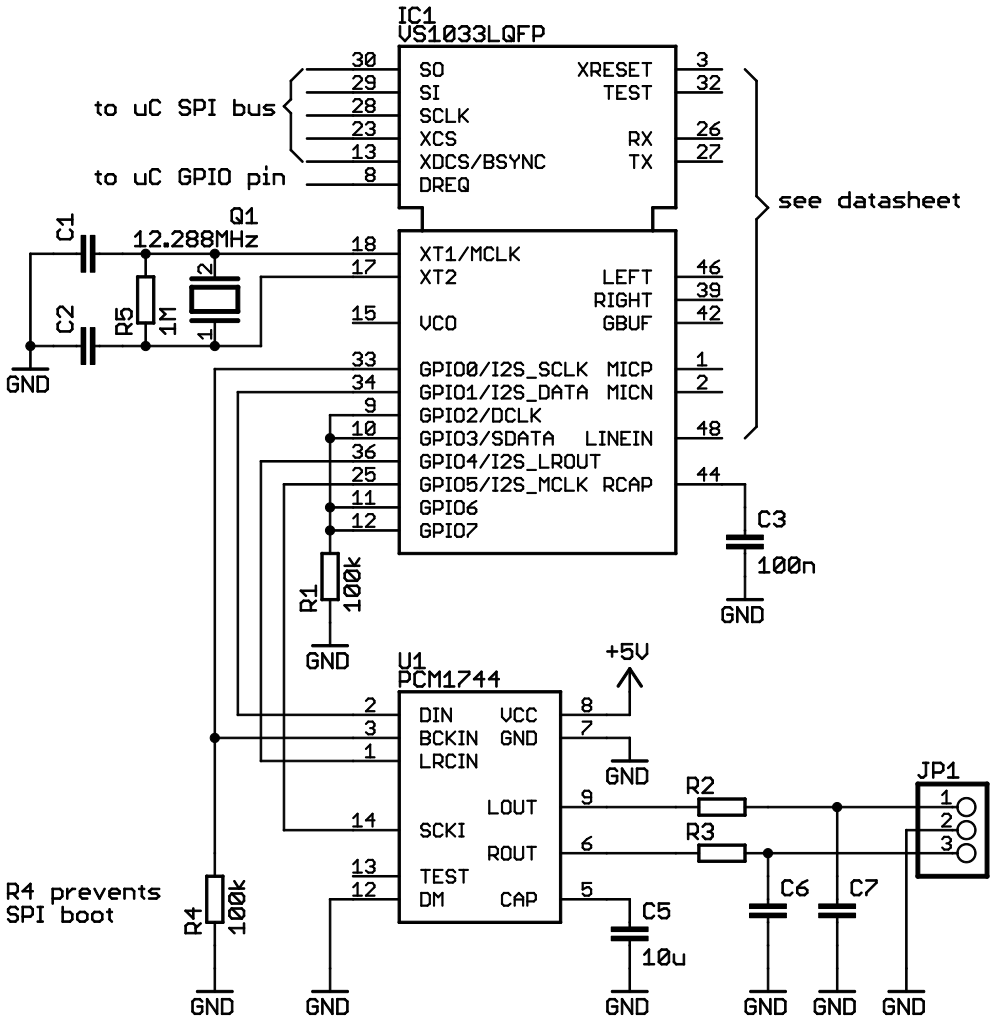

Figure 2: Example schematic using a PCM1744 DAC

4 Document Version Changes

This chapter describes the most important changes to this document.

Version 1.01, 2006-06-12

- Updated to VS1033.

Version 1.00, 2006-01-04

- Initial version.

5 Contact Information

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Note: If you have questions, first see
http://www.vlsi.fi/vs1011/faq/
http://www.vlsi.fi/vs1002/faq/
http://www.vlsi.fi/vs1003/faq/
http://www.vlsi.fi/appnotes