Ultra Low power Multiprocessor DSP core

Tampere, Finland, 19 March 2002 – VLSI Solution has announced the second generation of its ultra low power VS_DSP core processor.

VS_DSP^4 has the following major improvements over the old VS_DSP core:

- Double operation frequency
- Floating-point arithmetic requires half of the clock cycles (4x speed-up)
- Rounding instruction speeds up digital filtering
- Faster external memory access
- No power consumption penalty due to additional features
- No gate count penalty due to additional features
- C-level debugger added to the software tool set
- Multi-core support added to the software tools

A three-processor VS_DSP^4 cluster that provides 600 million MAC instructions per second requires less than 1 mm^2 silicon area in 0.18 µm technology and uses less than 30 mA (<50 µA/MHz/processor).

The software development kit is immediately available. The figure below shows the evaluation board for 3G portable platform with three processors, configurable logic and high-speed analog.

Like its predecessors, VS_DSP^4 is available as a VHDL soft core for licensing or as a building block for design service and manufacturing projects of VLSI Solution.

“The new processor makes it possible to implement cost and power effectively new real-time algorithms, such as MP3 encoding. Our symmetric parallel engine makes software development of parallel processors straightforward”, says Tapani Ritoniemi, Managing Director of VLSI Solution.

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