VS23S010D-S - 1 Megabit SPI SRAM
with Dual-I/O and Quad-I/O

Features

- Flexible 1.5V - 3.6V operating voltage
- 131,072 x 8-bit SRAM organization
- Serial Peripheral Interface (SPI) mode 0 compatible
  - Byte, Page and Sequential modes
  - Supports Single, Dual and Quad I/O read and write
  - Fast operation: the whole memory can be filled in 262158 or read in 262159 cycles (Quad-I/O SPI, Quad address mode)
  - XHOLD and XWP pins
- High operating frequencies
  - Up to 38 MHz for SPI
- Active Low-power
  - Read current 340 μA at 1 MHz (Single I/O, SO=0, T_A=+85°C, VDD=3.3V)
- Industrial temperature range
  - -40°C to + 85°C
- Pb-Free and RoHS compliant

Description

The VLSI Solution VS23S010D-S is an easy-to-use and versatile serial SRAM device. The memory is accessed via an SPI compatible serial bus.

Applications

- Micro-controller RAM extension
- VoIP and internet data stream buffer
- Audio data buffer

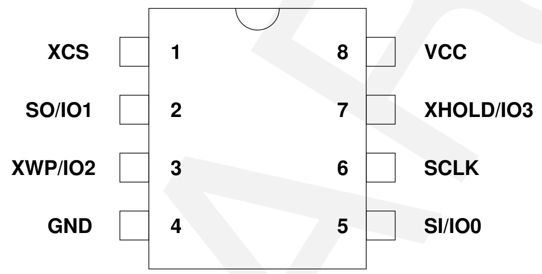


Figure 1: SOIC8 narrow package, compatible with standard pin out (not to scale).

Operating Modes

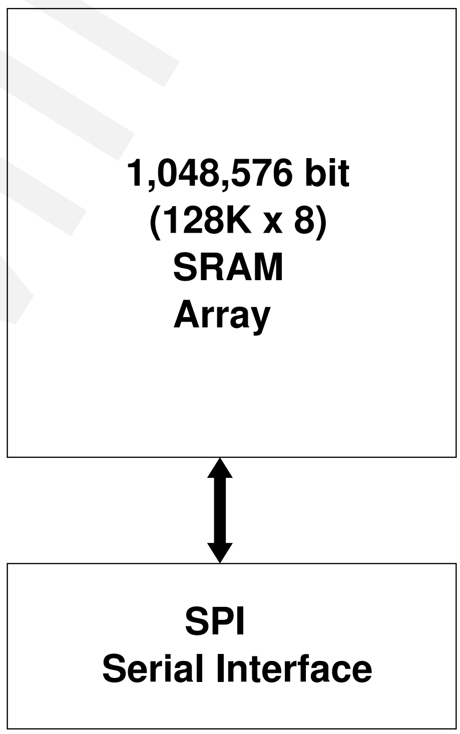
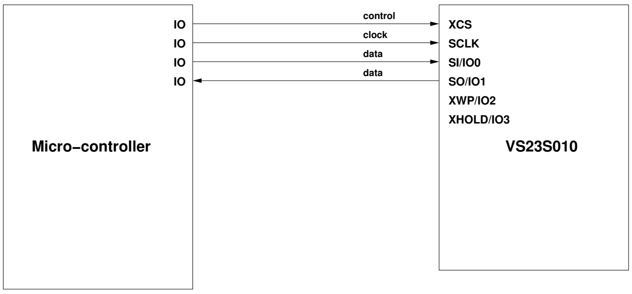


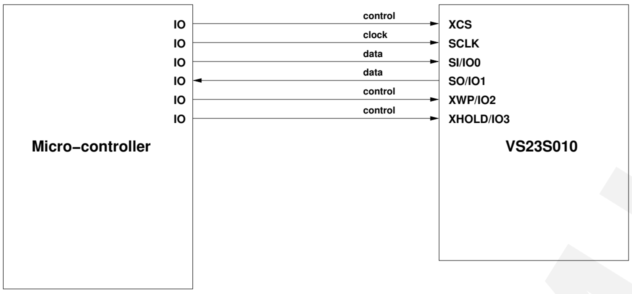
Figure 2: VS23S010D-S blocks

In SPI mode SRAM and control registers can be accessed. Dual-I/O and Quad-I/O modes are used only for SRAM read and write.

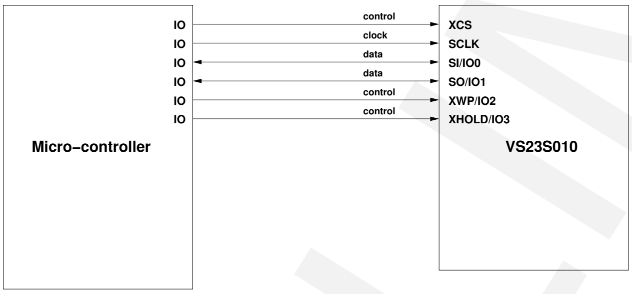
Following are connection examples for different operating modes. Some I/Os of VS23S010D-S are unconnected, because they have internal pull-up or pull-down resistors. Note also, that power and ground connections are not shown in the following examples.



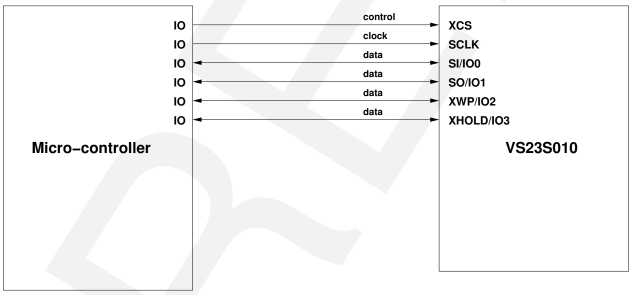
SPI connection, minimum configuration



SPI connection, basic configuration



SPI Dual−I/O connection



SPI Quad−I/O connection

Contents

List of Figures

1 Disclaimer

This is a *preliminary* data sheet. All properties and figures are subject to change.

2 Definitions

B Byte, 8 bits

b Bit

LSB Least Significant Bit

MSB Most Significant Bit

POR Power On Reset

SPI Serial Peripheral Interface

SRAM Static Random Access Memory

TBD To Be Defined

3 Electrical Characteristics & Specifications

3.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Positive Supply	VDD	-0.3	3.6	V
Current at any non-power pin[1]			±50	mA
Voltage at any digital input		-0.3	VDD+0.3[2]	V
Operating temperature		-40	+85	°C
Storage temperature		-65	+150	°C
ESD protection on any pin[3]		2.0		kV

[1] Higher current can cause latch-up.
[2] Must not exceed 3.6 V
[3] Human Body Model (HBM) MIL-STD-883E Method 3015.7

3.2 DC Characteristics

T_A = -40 ... +85 °C

Parameter	Min	Max	Unit	Test Conditions
Positive supply voltage	1.5	3.6	V	
High-level input voltage	$0.7\times$VDD	VDD+0.3[1]	V	
Low-level input voltage	-0.2	$0.3\times$VDD	V	
Low-level input voltage	-0.2	$0.25\times$VDD	V	Any Schmitt-trigger pin
High-level output voltage	$0.7\times$VDD		V	I_O = -1.0 mA
Low-level output voltage		$0.3\times$VDD	V	I_O = 1.0 mA
I/O leakage current [2]	-2.00	2.00	μA	Pin as input or High-Z
Pull-up current	-7.50	-1.00	μA	Any pull-up pin
I/O capacitance [3]		6	pF	VDD=0V, f=0.5 MHz, T_A=+25 °C
RAM data retention voltage [3,4]		0.9	V	
Start-up time after power-up [5]		100 [3]	μs	

[1] Must not exceed 3.6V
[2] Excluding the pins with pull-up or pull-down resistors
[3] This parameter is periodically sampled and is not 100% tested.
[4] This is the limit to which VDD can be lowered without losing RAM data.
[5] Refer to Chapter 8 for additional information.

3.3 AC Characteristics

3.3.1 General

VDD = 3.3 V, T_A = -40 ... +85 °C

Parameter	Symbol	Min	Max	Unit
Data clock high time	Tclkh	$0.5 * T_{MAX}$ [1]		ns
Data clock low time	Tclkl	$0.5 * T_{MAX}$ [1]		ns
Data clock rise time [2,3]	Tclkr		2	μs
Data clock fall time [2,3]	Tclkf		2	μs
Data in setup time	Tds	2		ns
Data in hold time	Tdh	6		ns
Output disable time [2]	Tdis		15	ns
Output valid time	Tv		30	ns
Output hold time	Toh	6		ns

[1] T_{MAX} is the minimum clock cycle time in each mode.
[2] This parameter is periodically sampled and is not 100% tested.
[3] Refer to Chapter 8 for additional information.

3.3.2 SPI Mode

VDD = 3.3 V, T_A = -40 ... +85 °C

Parameter	Symbol	Min	Max	Unit	Test Conditions
SPI clock frequency [1]	F_{SCLK}		32 38	MHz MHz	VDD = 1.5 V VDD $\geq$ 1.8 V
XCS high time	Txcshi	31 26		ns ns	VDD = 1.5 V VDD $\geq$ 1.8 V
XCS setup time	Txcss	4		ns	
XCS hold time	Txcsh	0		ns	
XHOLD setup time	Txhs	2		ns	
XHOLD hold time	Txhh	1		ns	
XHOLD low to output High-Z [2]	Txhlz	4		ns	
XHOLD high to output valid [2]	Txhhz		16	ns	
XWP setup time	Txws	1		ns	
XWP hold time	Txwh	1		ns	

[1] When used with an external micro-controller the maximum SPI frequency is based on the total of VS23S010D-S and micro-controller I/O-delays and routing delays of the card.
[2] This parameter is periodically sampled and is not 100% tested.

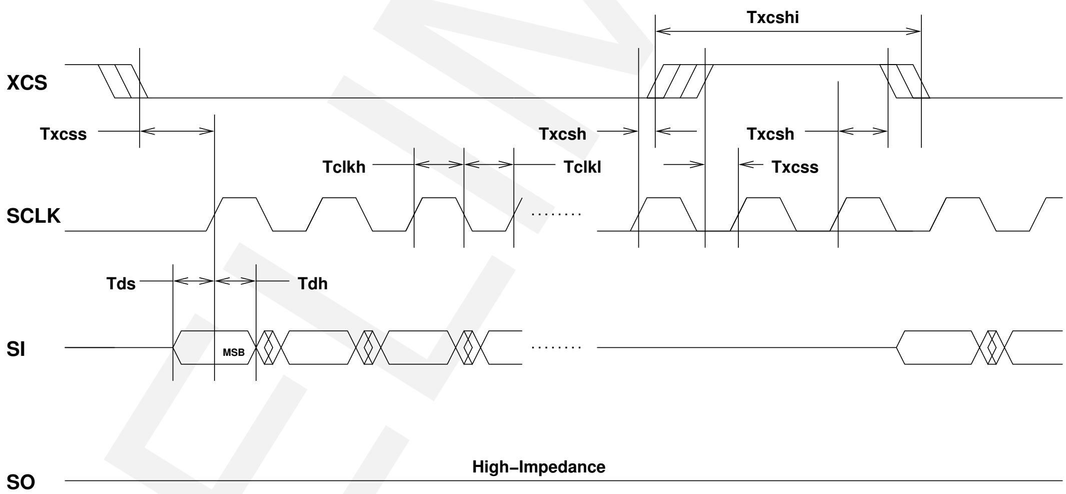


Figure 3: SPI Input Timing

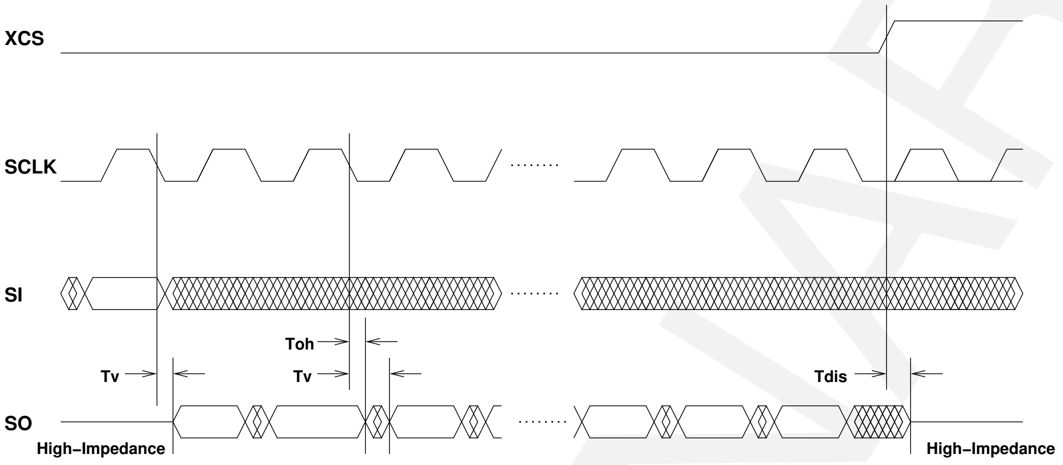


Figure 4: SPI Output Timing

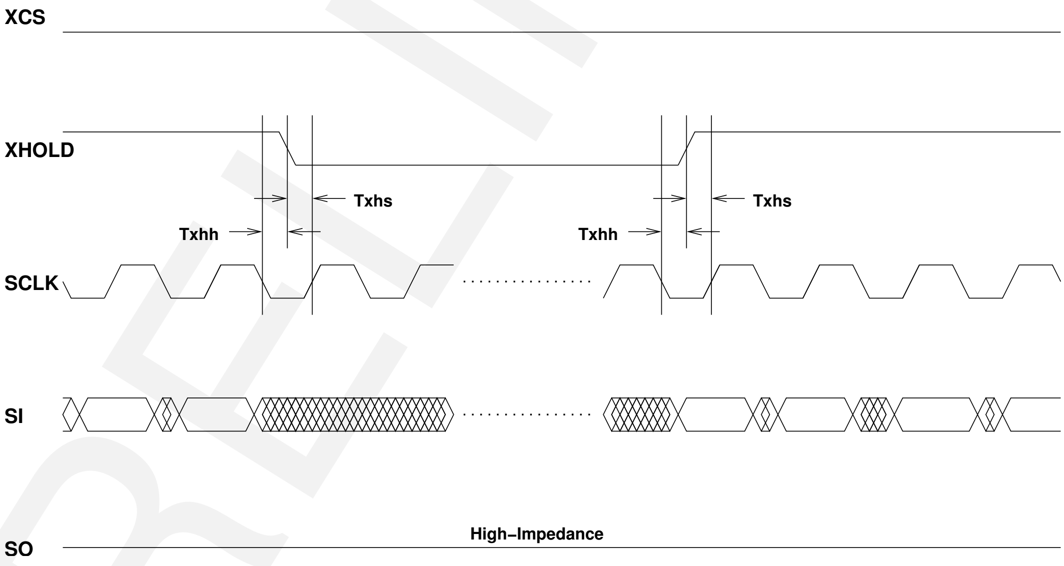


Figure 5: XHOLD Timing, SPI and Dual-I/O Input Modes. Notice that internal address counter does not increment, when XHOLD is low.

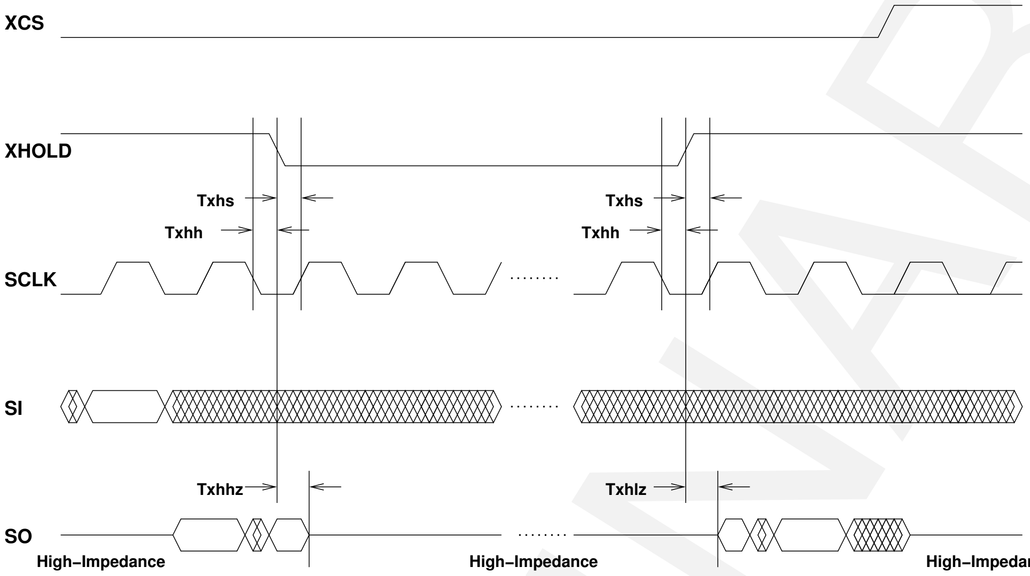


Figure 6: XHOLD Timing, SPI and Dual-I/O Output Modes. Notice that internal address counter does not increment, when XHOLD is low.

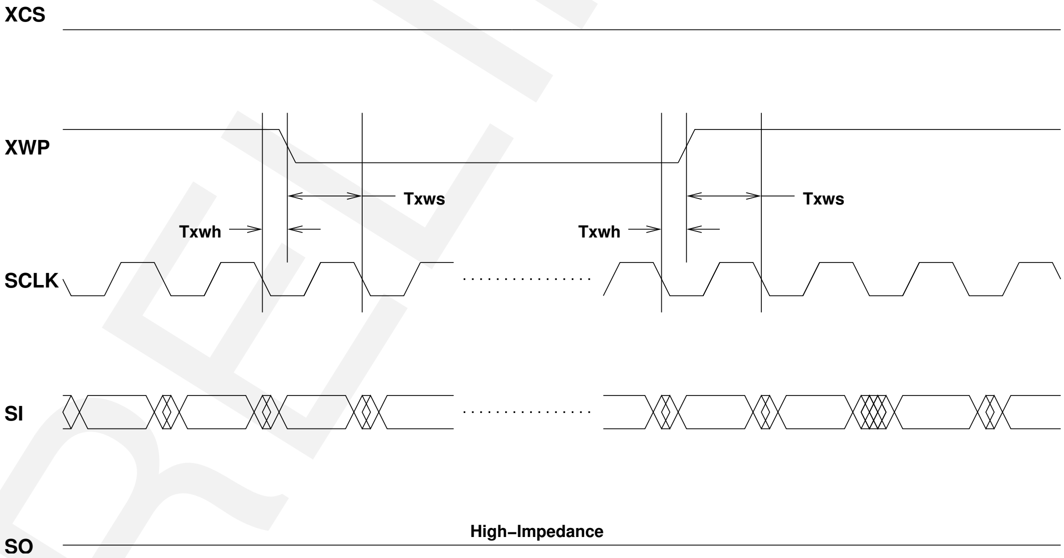


Figure 7: XWP Timing, SPI and Dual-I/O Modes. Notice that internal address counter increments, when XWP is low.

AC Test Conditions

AC Waveform:	
Input pulse level	$0.1\times$VDD to $0.9\times$VDD
Input rise/fall time	(TBD) ns
Operating temperature	-40 °C to +85 °C
C_L = (TBD) pF	
Timing Measurement Reference Level:	
Input	$0.5\times$VDD
Output	$0.5\times$VDD

3.4 Current Consumption

T_A = +25 °C, XCS=VDD, SI=SO=SCLK=GND, other inputs connected to VDD or GND by on-chip pull-up or pull-down resistors of the pins.

Parameter	Min	Typ	Max	Unit	Test Conditions
Stand-by current [1]		40-65	(TBD)	µA	
			300 [2]	µA	T_A = +85 °C
			1000 [2]	µA	T_A = +125 °C

[1] Additional information is in Chapter 8
[2] This parameter is periodically sampled and is not 100% tested.

3.4.1 SPI Mode

VDD = 3.3 V, T_A = +85 °C, these parameters are periodically sampled and are not 100% tested.

Parameter	Min	Typ	Max	Unit	Test Conditions
VDD current, SPI single output read			340	µA	F_{SCLK} = 1 MHz, SO = 0
			740	µA	F_{SCLK} = 10 MHz, SO = 0
			1.3	mA	F_{SCLK} = 24 MHz, SO = 0
VDD current, SPI single port write & read, two patterns[1]		0.1-1.3		mA	F_{SCLK} = 1 MHz, T_A = +25 °C
		1.0-2.7		mA	F_{SCLK} = 10 MHz, T_A = +25 °C

[1] Current is very much data-dependent.

4 Packages and Pin Descriptions

4.1 Narrow SOIC8

Narrow SOIC8 is a lead (Pb) free and also RoHS compliant package. RoHS is a short name of *Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment*.

Narrow SOIC8 package dimensions can be found at *http://www.vlsi.fi/fileadmin/quality/soic8.pdf*.

The VS23S010D-S has the following pin out:

Pin Name	SOIC8 Pin	Pin Type	Function	Initial State
XCS	1	DIS	Active low chip select for SPI	I
SO/IO1	2	DIO	SO for SPI / IO1 for Dual-I/O and Quad-I/O SPI	I
XWP/IO2	3	DIOSPU	Active low write protect for SPI and Dual-I/O SPI / IO2 for Quad-I/O SPI	IH
GND	4	GND	Ground	
SI/IO0	5	DIO	SI for SPI / IO0 for Dual-I/O and Quad-I/O SPI	I
SCLK	6	DIS	SCLK for SPI	I
XHOLD/IO3	7	DIOSPU	Active low Hold for SPI and Dual-I/O SPI / IO3 for Quad-I/O SPI	IH
VCC	8	PWR	Power supply	

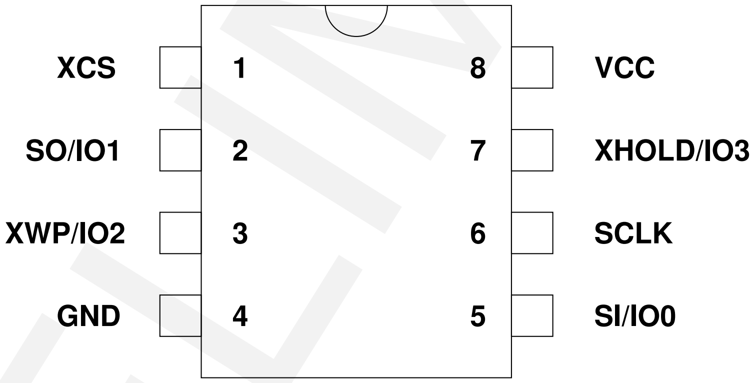


Figure 8: SOIC8 narrow package, compatible with standard pin out (not to scale).

Pin types:

Type	Description
DIS	Digital input, Schmitt-trigger
DIO	Digital input/output
DIOSPU	Digital input/output with Pull-Up resistor, Schmitt-trigger
GND	Ground pin
PWR	Power supply pin

Initial States of pins after power-up:

Initial State	Description
I	Input, floating (3-state)
IH	Input, on-chip Pull-Up resistor

5 Connection Guidelines

To minimize power supply noise connect suitable by-pass capacitors between VCC supply pins and GND. Place by-pass capacitors as near as possible to VS23S010D-S for best effect.

Make sure that there is the lowest possible capacitive coupling between different clocks and chip selects (SCLK and XCS) and particularly to data signals on the circuit board. This is for minimizing interference between these signals.

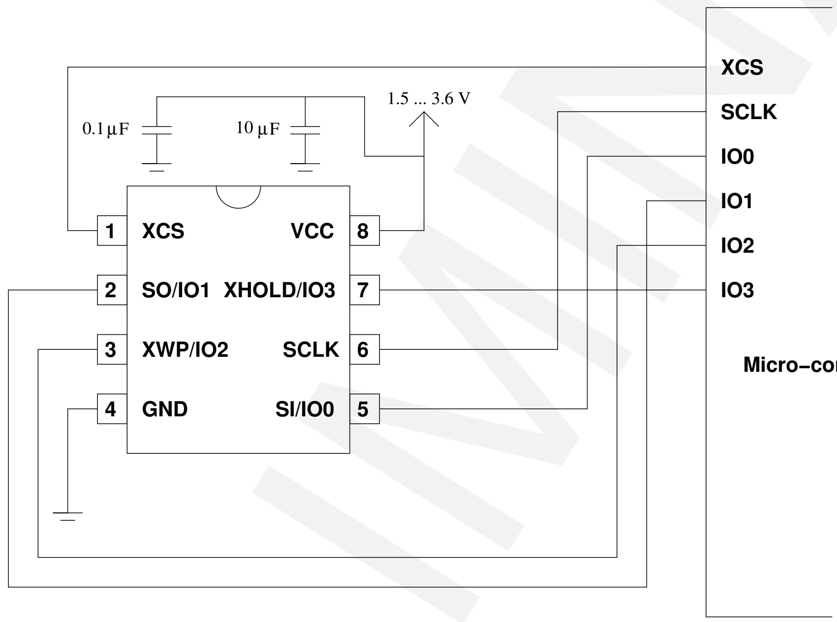


Figure 9: Connection example

6 Device Operation

The device consists of following main blocks: SPI and SRAM.

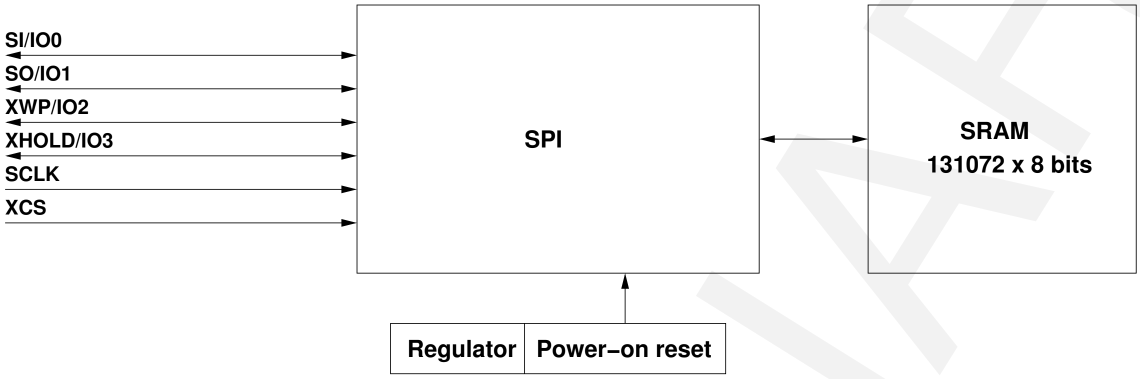


Figure 10: Device Organization

6.1 SPI

The VS23S010D-S is controlled by a set instructions that are sent from a host controller, commonly referred as SPI Master. The SPI Master communicates with the VS23S010D-S via the SPI bus which is comprised of four signal groups: Chip Select (XCS), Serial Clock (SCLK), Serial Input (SI, also SO in Dual-I/O mode and XWP and XHOLD in Quad-I/O mode) and Serial Output (SO, also SI in Dual-I/O mode and XWP and XHOLD in Quad-I/O mode).

The VS23S010D-S supports SPI protocol operation mode 0, which is very commonly used. Data is always latched in on the rising edge of the SCLK and always output on the falling edge of the SCLK. SPI mode 0 is used in Single, Dual-I/O and Quad-I/O modes.

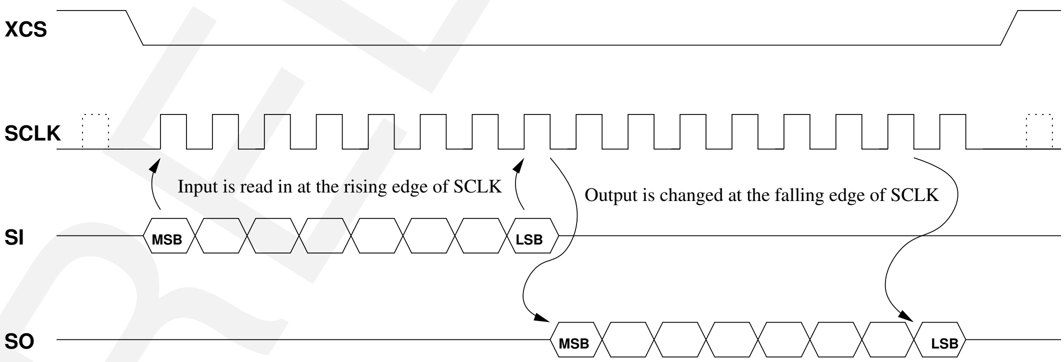


Figure 11: SPI Mode 0

SPI block does not have a separate Reset pin. There is an on-chip power-up delay logic, which is used to reset the selected SPI registers. SPI block logic is clocked by the SCLK pin. Following is a table describing the registers of the VS23S010D-S.

Register	Symbol	R/W	Default Value	Initialization
General				
Status	STATUS	RW	00h	Power-Up
Manufacturer and Device ID	ID	R	ABh	Power-Up

6.1.1 Word, Page and Sequential Operation Modes

Bits 7 to 6 of the Status register select these three SPI Operation Modes. These modes affect SPI Single, Dual and Quad I/O SRAM operations.

Byte Operation This mode is selected when Mode bits are “00”. Read and write operations are limited to one byte in this mode i.e. address does not increment after each written or read byte. After command and 24-bit address byte data is read from or written to given SRAM address every time after subsequent 8 (Single), 4 (Dual-I/O) or 2 (Quad-I/O) SCLK cycles.

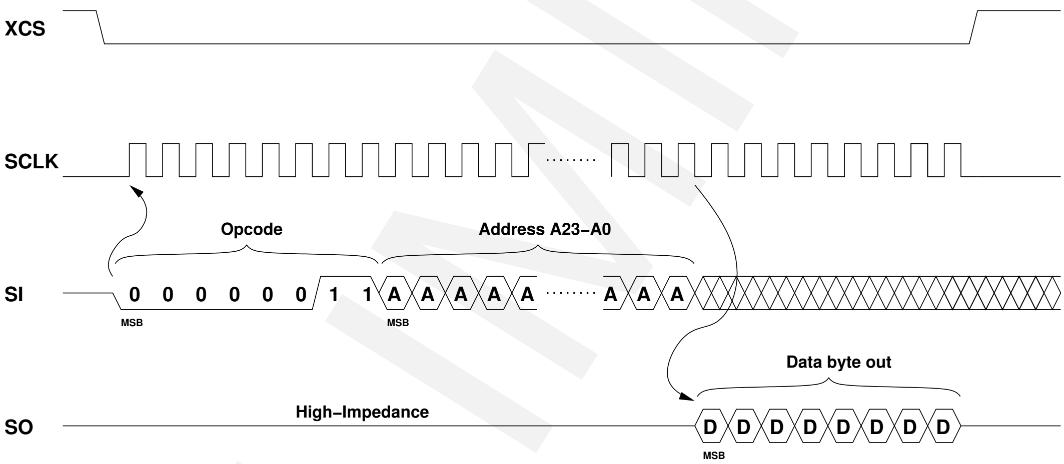


Figure 12: SPI Byte read

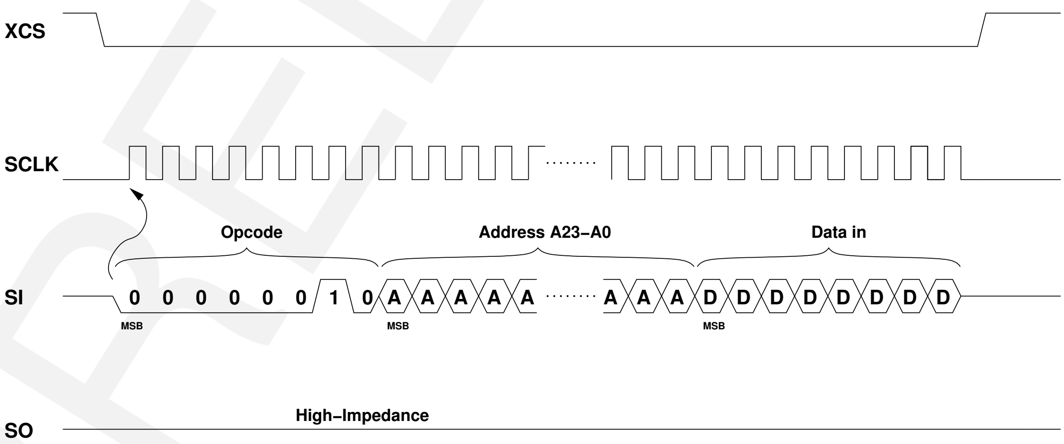


Figure 13: SPI Byte write

Page Operation This mode is selected when Mode bits are "10". VS23S010D-S has 4096 pages of 32 bytes. In page mode reads and writes are limited to the page selected by the given address. After each written or read byte the SRAM address is increased automatically. When the last address of page is reached the accessing will continue from the first address of the page.

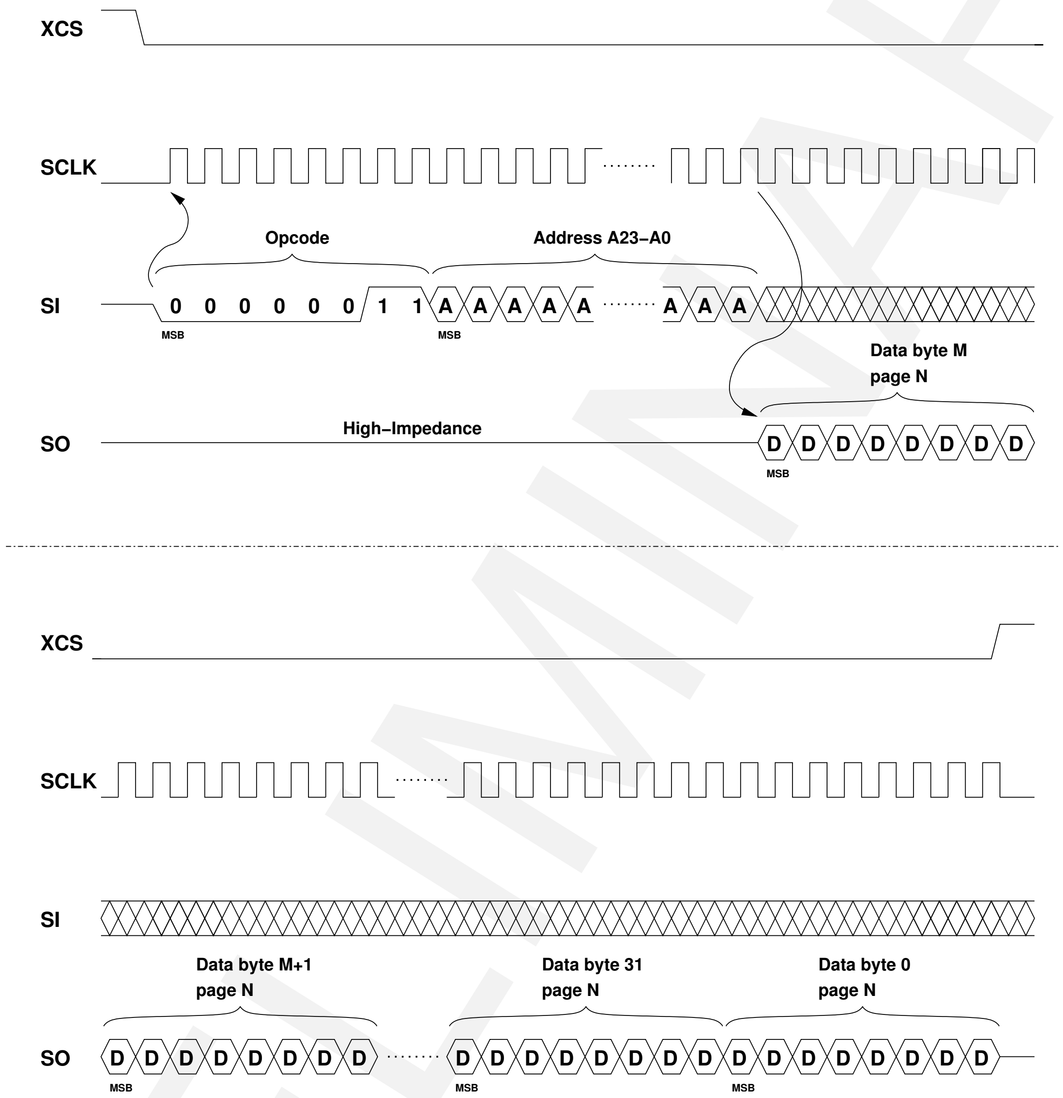


Figure 14: SPI Page read

Sequential Operation This mode is selected when Mode bits are "01". In this mode the entire SRAM array can be accessed in one operation. The address counter is increased automatically and when the last address 1FFFFh of the SRAM is reached the address counter returns to value 00000h.

If several VS23S010D-Ss are connected to SPI or 8-bit parallel bus in Multi-IC configuration, in the case of address wrapping around the addressing continues from the address 00000h of the next VS23S010D-S in system.

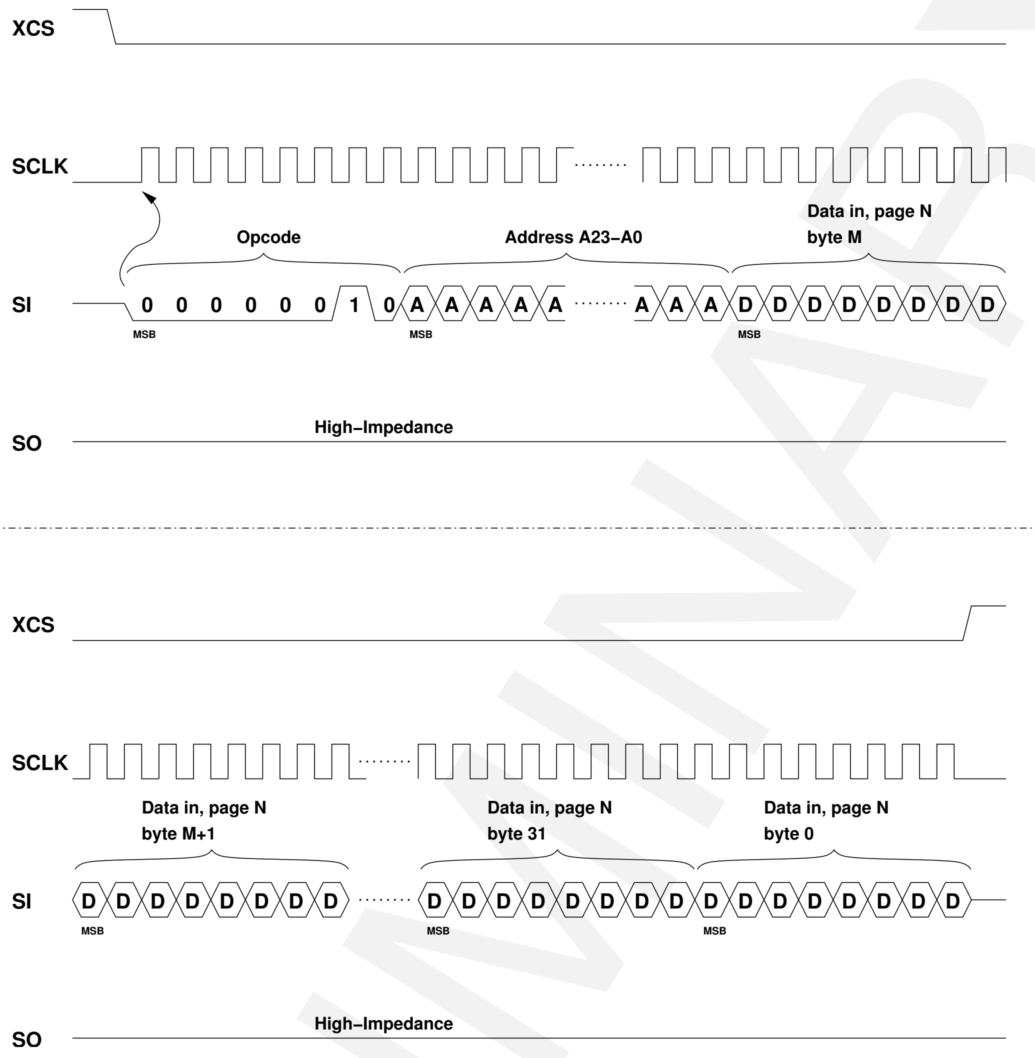


Figure 15: SPI Page write

6.1.2 Dual-I/O and Quad-I/O Operation

In Dual-I/O SPI mode two data bits are read or written during one SCLK cycle. SI/IO0 pin is the lower bit and SO/IO1 pin is the higher bit in Dual-I/O mode. Both pins are inputs during the write and outputs during the read.

In Quad-I/O SPI mode four data bits are read or written during one SCLK cycle. SI/IO0 pin is the lowest bit, SO/IO1 pin is the second bit, XWP/IO2 is the third bit and finally XHOLD/IO3 is the fourth bit in Quad-I/O mode. The pins are inputs during the write and outputs during the read.

In these modes the SPI command is still given in one-bit SPI mode. The address can be given either in one-bit SPI mode or multi-bit SPI mode depending on the given command.

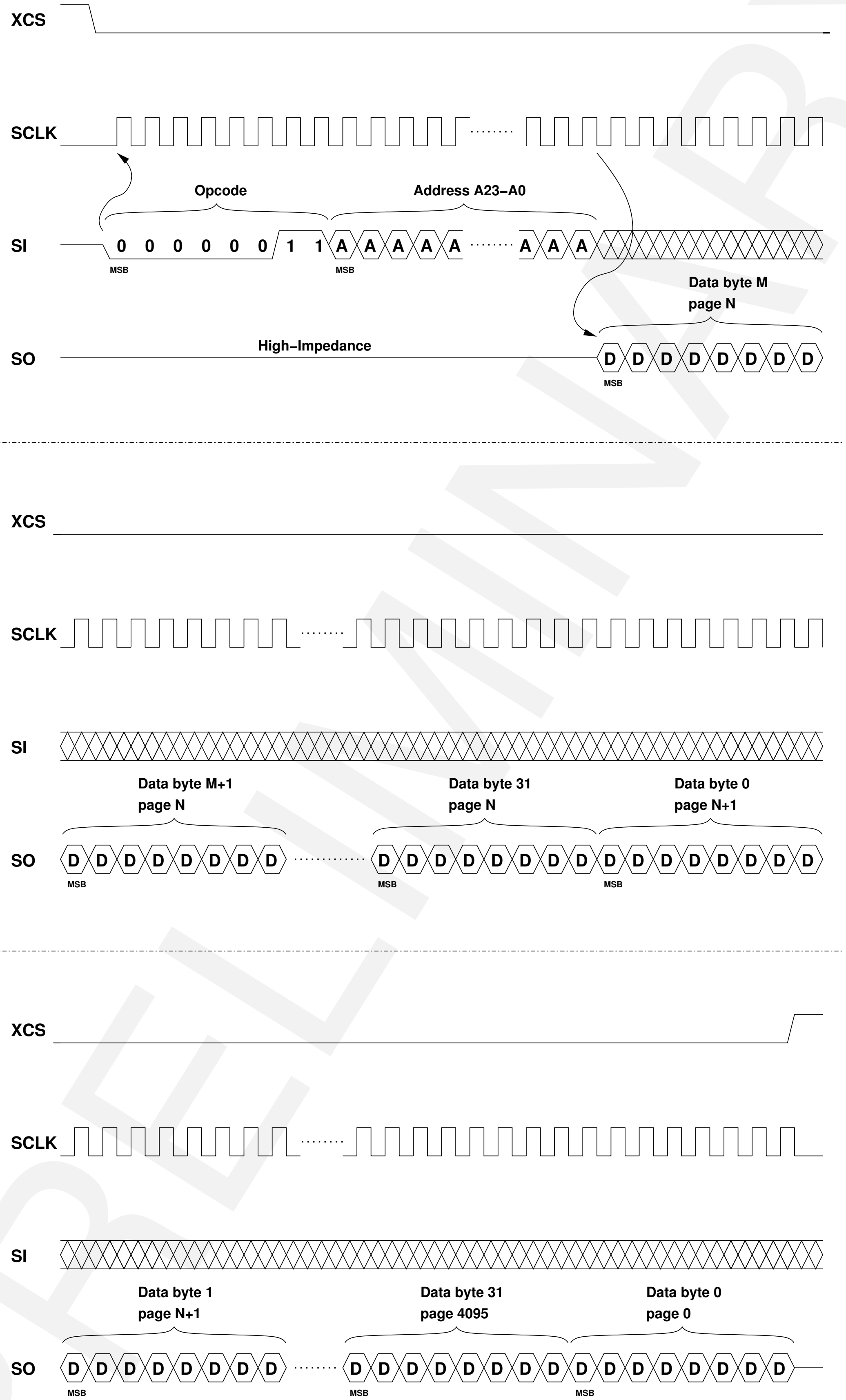


Figure 16: SPI sequential read

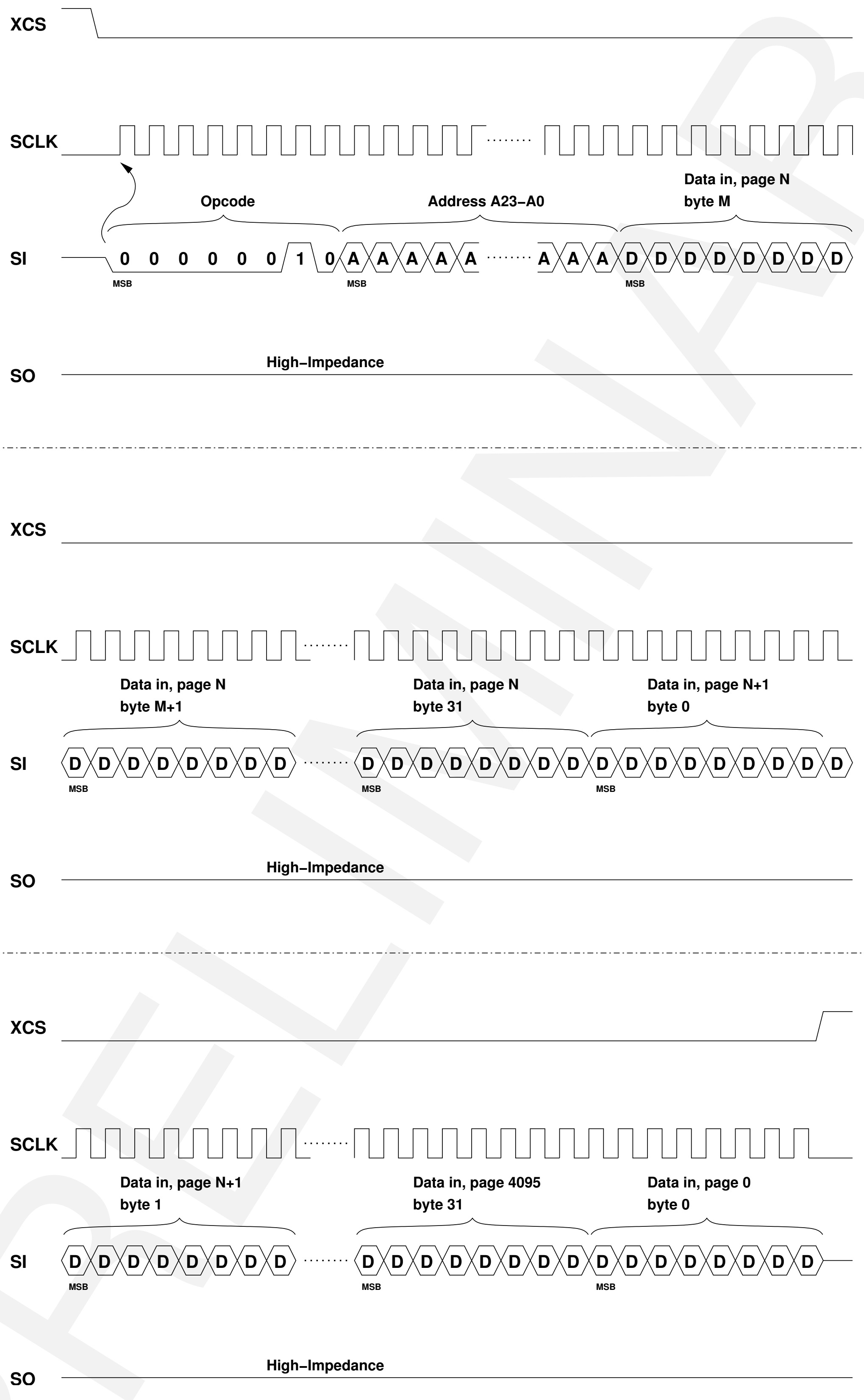


Figure 17: SPI sequential write

6.1.3 Write Protect in Single- and Dual-I/O Modes

In single and dual-I/O modes it is possible to suspend writing of some bits during the write operation. This is done by setting XWP pin to low state when SCLK pin is low. When the XWP pin is low SPI data is not taken into VS23S010D-S even though SCLK is toggled. The address counter is incremented during this time when SCLK is toggled like normally in write operation. When the XWP pin is set to high during SCLK low state the write operation continues to an updated SRAM address.In Figure 7 is shown XWP timing.

6.1.4 Hold in Single- and Dual-I/O Modes

Hold functionality can be enabled by writing the StSPIH bit of Status register high. After VS23S010D-S power-up the StSPIH bit is low and Hold function is disabled.

XHOLD pin can be used in single and dual-I/O memory operations. Setting XHOLD low in these modes suspends the operation in progress (SPI read or write). The state of the XHOLD pin can be changed when SCLK is in low state. When XHOLD is low during SPI memory operation the SRAM address counter does not increment even though SCLK is toggled. In read operation the SO output goes to high-impedance state when XHOLD is low. This allows SPI bus to be used by some other device during the VS23S010D-S memory operation. When the XHOLD pin is set to high again the VS23S010D-S memory operation continues. In Figures 5 and 6 are shown hold functionality.

7 SPI Commands and Addressing

A valid SPI instruction or operation is started by first asserting the XCS pin. After that, the host controller clocks out a valid 8-bit opcode on the SPI bus. Following the opcode instruction dependent information (address or data bytes) is sent by the host controller. Address and data are sent MSB first. Operation is ended by deasserting the XCS pin.

Opcodes which are not supported by the VS23S010D-S are not allowed . Also if XCS is deasserted when the whole byte is not clocked out the operation of the byte in question will be aborted.

Addressing the SRAM of the VS23S010D-S requires three bytes to be sent, address bits A23-A0. Since the maximum address of one VS23S010D-S is 1FFFFh the address bits A16 to A0 will be used by one device. Address bits A23 to A17 are ignored by the VS23S010D-S.

Command	Opcode		Address Bytes	Data Bytes
SRAM Read Commands				
Read	03h	0000 0011	3	1+
Dual-Output Read	3Bh	0011 1011	3	1+
Dual-Output Read, Dual Address	BBh	1011 1011	3	1+
Quad-Output Read	6Bh	0110 1011	3	1+
Quad-Output Read, Quad Address	EBh	1110 1011	3	1+
SRAM Write Commands				
Write	02h	0000 0010	3	1+
Dual-Input Write	A2h	1010 0010	3	1+
Dual-Input Write, Dual Address	22h	0010 0010	3	1+
Quad-Input Write	32h	0011 0010	3	1+
Quad-Input Write, Quad Address	B2h	1011 0010	3	1+
Miscellaneous Commands				
Read Status Register	05h	0000 0101	0	1+
Write Status Register	01h	0000 0001	0	1+
Read Manufacturer and Device ID	9Fh	1001 1111	0	1+

7.1 SPI Read Commands (03h)

The Read command can be used to sequentially read a continuous stream data from the device by providing clock signal once the initial starting address has been specified. The device has on internal address counter that increments or not on every cycle depending on SPI operating mode.

To perform a read operation, XCS must first be asserted and read opcode must be clocked into device. After the opcode three address bytes are clocked into the device to specify the starting address location of the first byte to read within SRAM.

After address bytes additional SCLK clock cycles will result in data being output on the SO pin. Data is output MSB first. In sequential mode when the last byte (1FFFFh) of the SRAM has been read, the reading will continue from the beginning of the array (00000h). However, if there are several VS23S010D-Ss in Multi-IC configuration and sequential mode is selected, the reading will continue from the beginning of the array (00000h) of the next VS23S010D-S device. Also, if last VS23S010D-S accesses its last byte (1FFFFh) in Multi-IC mode, the reading will continue from the beginning of the array (00000h) of the first VS23S010D-S device.

Deasserting the XCS pin will terminate the read operation and SO pin goes to high-impedance state.

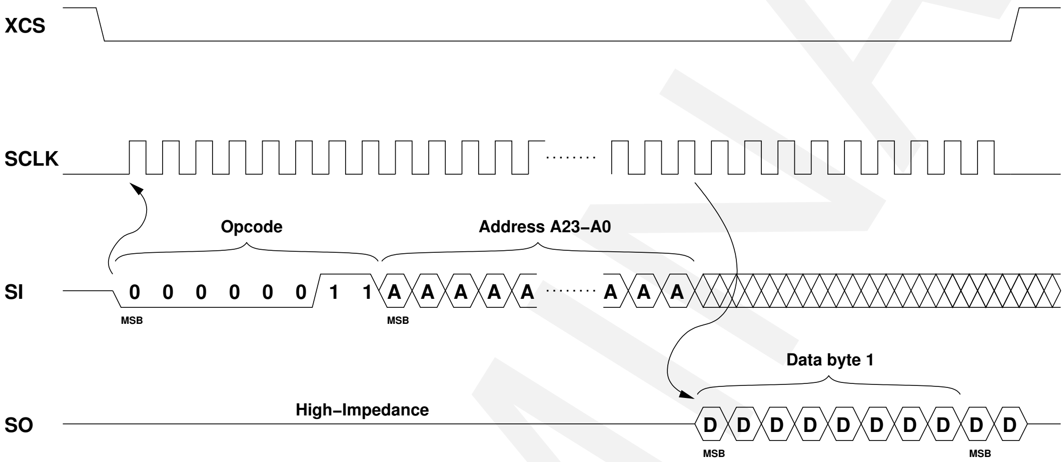


Figure 18: SPI Read

7.1.1 Dual-Output Read (3Bh and BBh)

Dual-Output Read is similar to Read command except that two bits of data are clocked out of the device on every clock cycle.

To perform a Dual-Output Read XCS pin is first asserted. After that opcode 3Bh and three address bytes are sent by the host controller.

After the three address bytes are clocked in, the device will output data on SI/IO0 and SO/IO1 pins. The data is clocked out MSB first and MSB is on pin SO/IO1. During the first clock cycle bit6 will be on SI/IO0 pin, on the next cycle bit5 is on SO/IO1 and bit4 on SI/IO0 and so on. In sequential mode the SRAM addressing will roll over similarly to normal SPI read operation.

Deasserting the XCS pin will terminate the read operation and SI/IO0 and SO/IO1 pins go to high-impedance state.

Dual-Output, Dual Address Read is similar to Dual-Output Read command except that two bits of address are clocked in the device on every clock cycle.

To perform a Dual-Output, Dual Address Read XCS pin is first asserted. After that opcode BBh

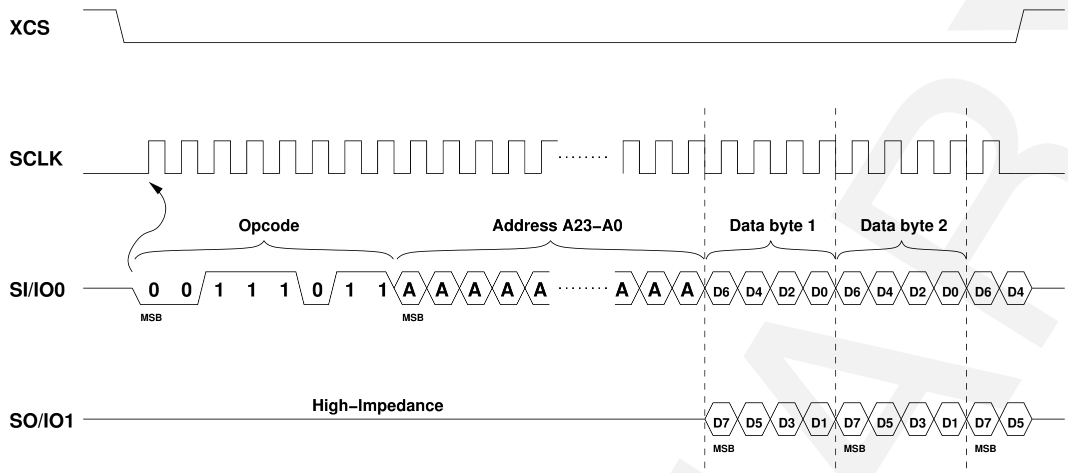


Figure 19: SPI Dual-Output Read

is sent in one bit mode and three address bytes are sent in dual I/O mode by the host controller to SI/IO0 and SO/IO1 pins.

After the three address bytes are clocked in, there is a dummy byte cycle. After that the device will output data on SI/IO0 and SO/IO1 pins. The rest of the operation is similar to Dual-Output Read.

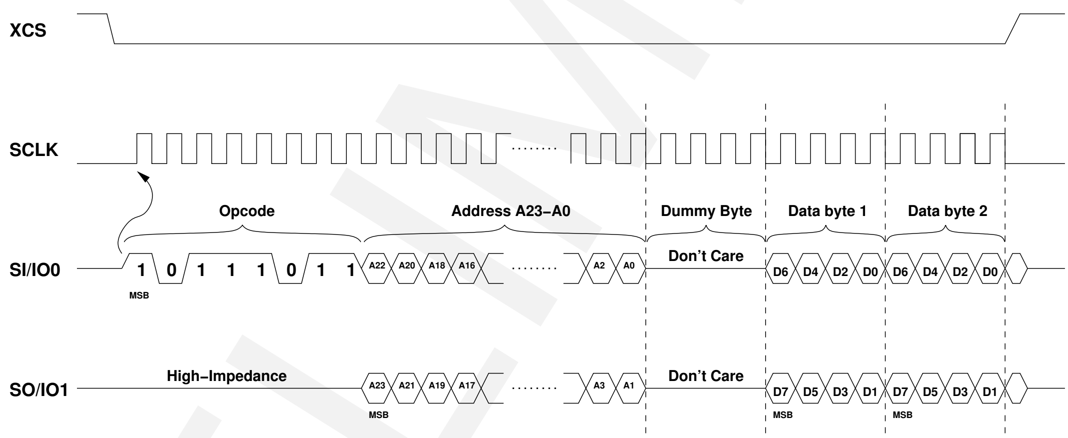


Figure 20: SPI Dual-Output Read, Dual Address

7.1.2 Quad-Output Read (6Bh and EBh)

Quad-Output Read is similar to Read command except that four bits of data are clocked out of the device on every clock cycle.

To perform a Quad-Output Read XCS pin is first asserted. After that opcode 6Bh and three address bytes are sent by the host controller.

After the three address bytes are clocked in, the device will output data on SI/IO0, SO/IO1, XWP/IO2 and XHOLD/IO3 pins. The data is clocked out MSB first and MSB is on pin XHOLD/IO3.

During the first clock cycle bit6 will be on XWP/IO2 pin, bit5 on pin SO/IO1 and bit4 on SI/IO0, on the next cycle bit3 is on XHOLD/IO3 and bit2 on XWP/IO2 and so on. In sequential mode the SRAM addressing will roll over similarly to normal SPI read operation.

Deasserting the XCS pin will terminate the read operation and SI/IO0, SO/IO1, XWP/IO2 and XHOLD/IO3 pins go to high-impedance state.

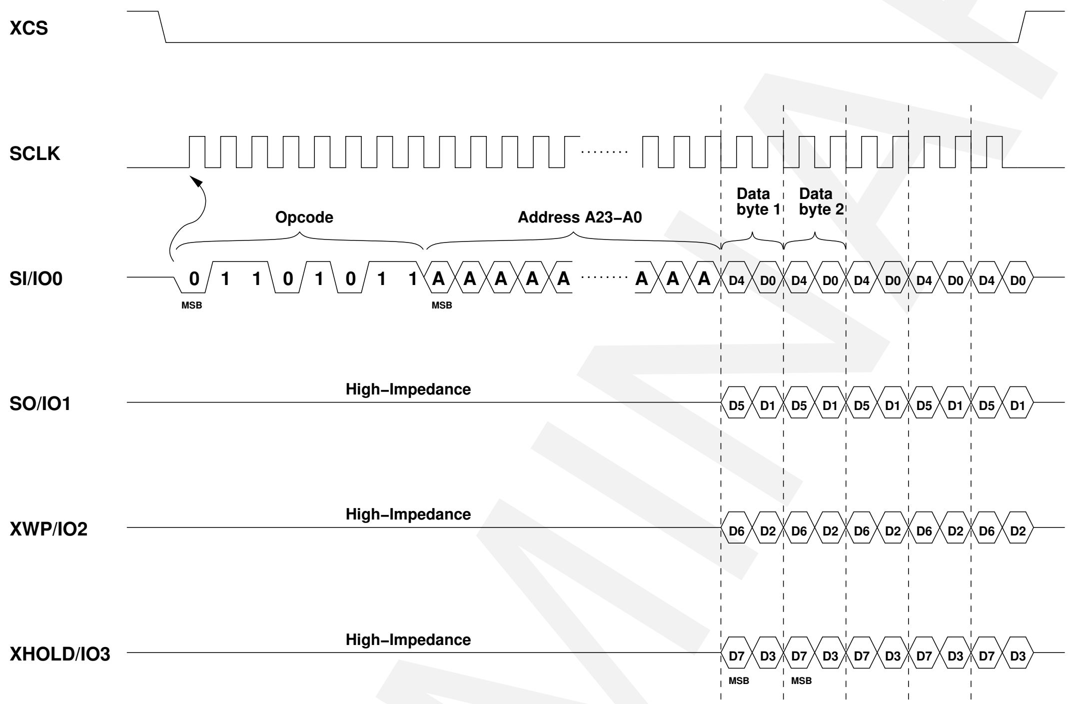


Figure 21: SPI Quad-Output Read

Quad-Output, Quad Address Read is similar to Quad-Output Read command except that four bits of address are clocked in the device on every clock cycle.

To perform a Quad-Output, Quad Address Read XCS pin is first asserted. After that opcode EBh is sent in one bit mode and three address bytes are sent in quad I/O mode by the host controller to SI/IO0, SO/IO1, XWP/IO2 and XHOLD/IO3 pins.

After the three address bytes are clocked in, there is a dummy byte cycle. After that the device will output data on SI/IO0, SO/IO1, XWP/IO2 and XHOLD/IO3 pins. The rest of the operation is similar to Quad-Output Read.

7.2 SPI Write Commands (02h)

Prior to writing the device must be selected by bringing XCS pin low. Once the device is selected the Write command can be started by issuing a Write instruction (opcode 02h) followed by a 23-bit address. If the device works in sequential mode (set by Status Register write) then after the initial data byte additional bytes can be clocked into device. The internal address pointer is automatically incremented when needed depending on operating mode. In sequential

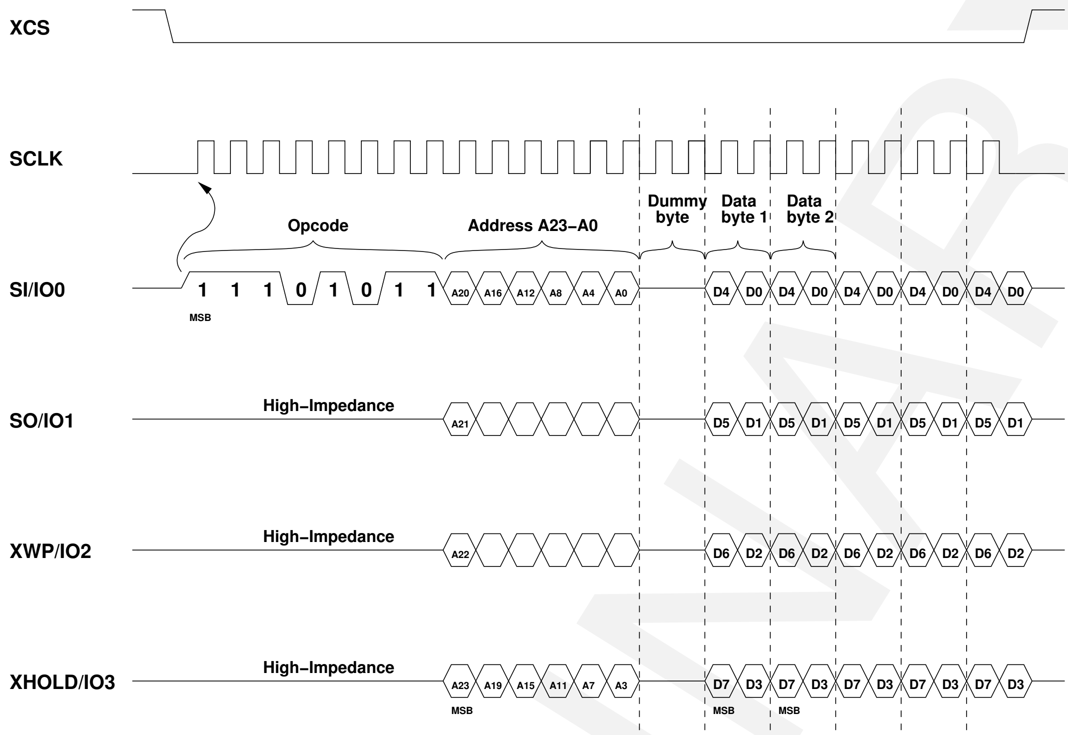


Figure 22: SPI Quad-Output Read, Quad Address

mode when the internal address pointer reaches its maximum value (1FFFFh) it rolls over to 00000h. If VS23S010D-S is part of the Multi-IC setup, then in sequential mode the writing will continue from the beginning (00000h) of the next VS23S010D-S SRAM. Also in sequential mode after the last byte (1FFFFh) of the last VS23S010D-S is written, the writing continues from the beginning (00000h) of the first VS23S010D-S SRAM. This allows the operation to continue indefinitely, however, previous data will be overwritten.

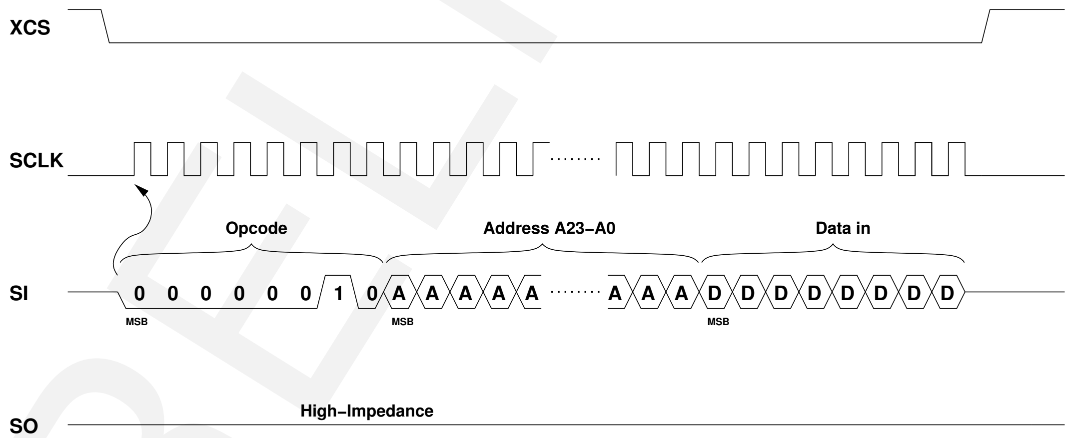


Figure 23: SPI Write

7.2.1 Dual-Input Write (A2h and 22h)

Dual-Input Write command is similar to Write command except that two bits of data are clocked in the device on every clock cycle and opcode is A2h.

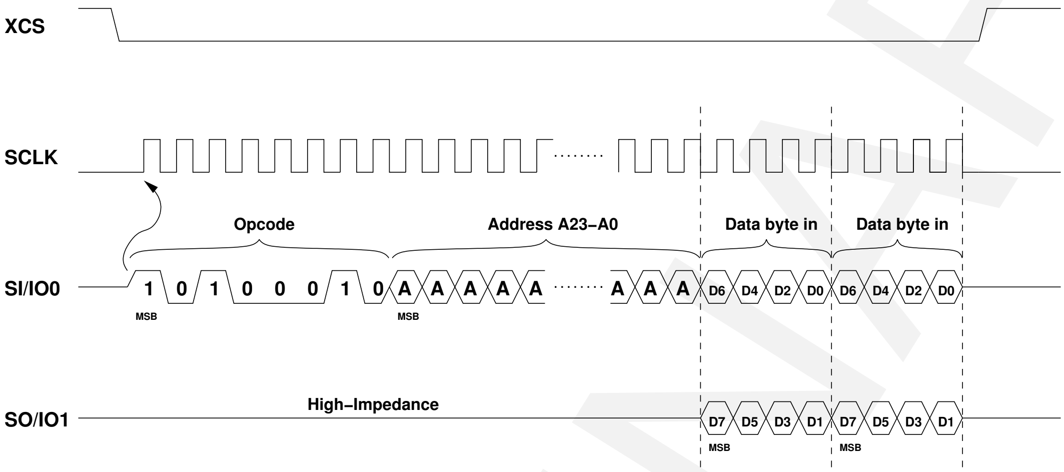


Figure 24: SPI Dual-Input Write

Dual-Input, Dual Address Write command is similar to Dual-Input Write command except that two bits of address are clocked in the device on every clock cycle and opcode is 22h.

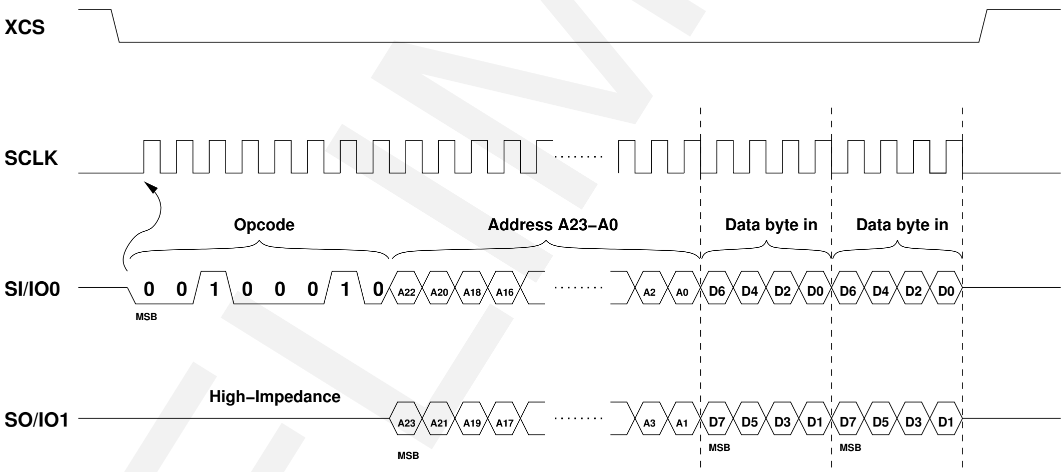


Figure 25: SPI Dual-Input, Dual Address Write

7.2.2 Quad-Input Write (32h and B2h)

Quad-Input Write command is similar to Write command except that four bits of data are clocked in the device on every clock cycle and opcode is 32h.

Quad-Input, Quad Address Write command is similar to Quad-Input Write command except that four bits of address are clocked in the device on every clock cycle and opcode is B2h.

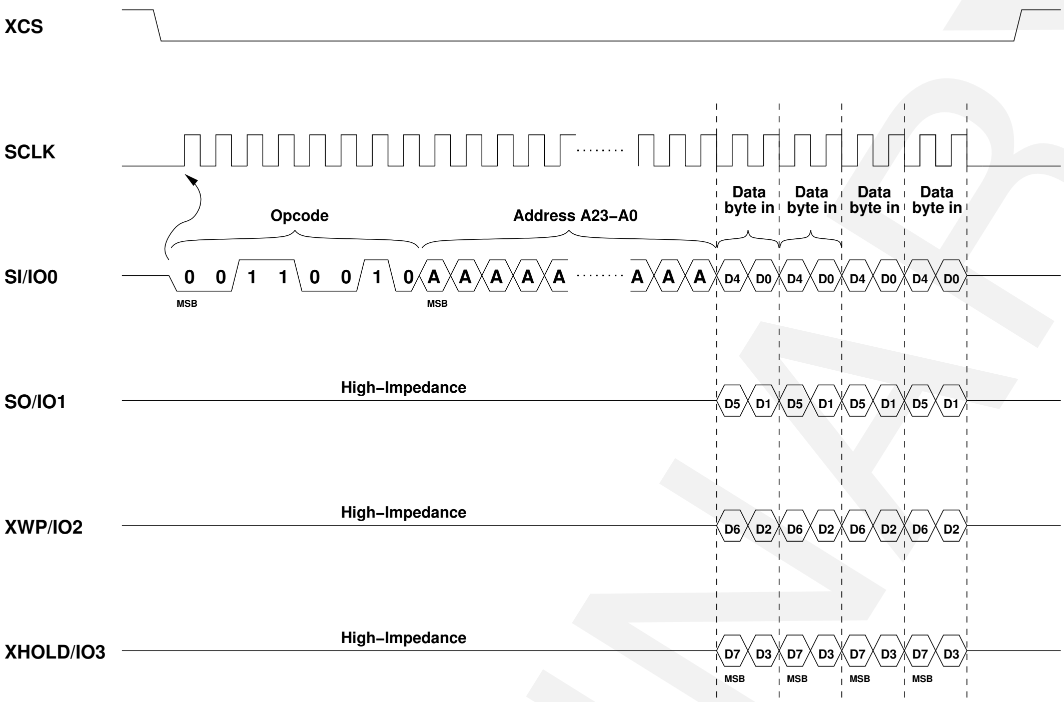


Figure 26: SPI Quad-Input Write

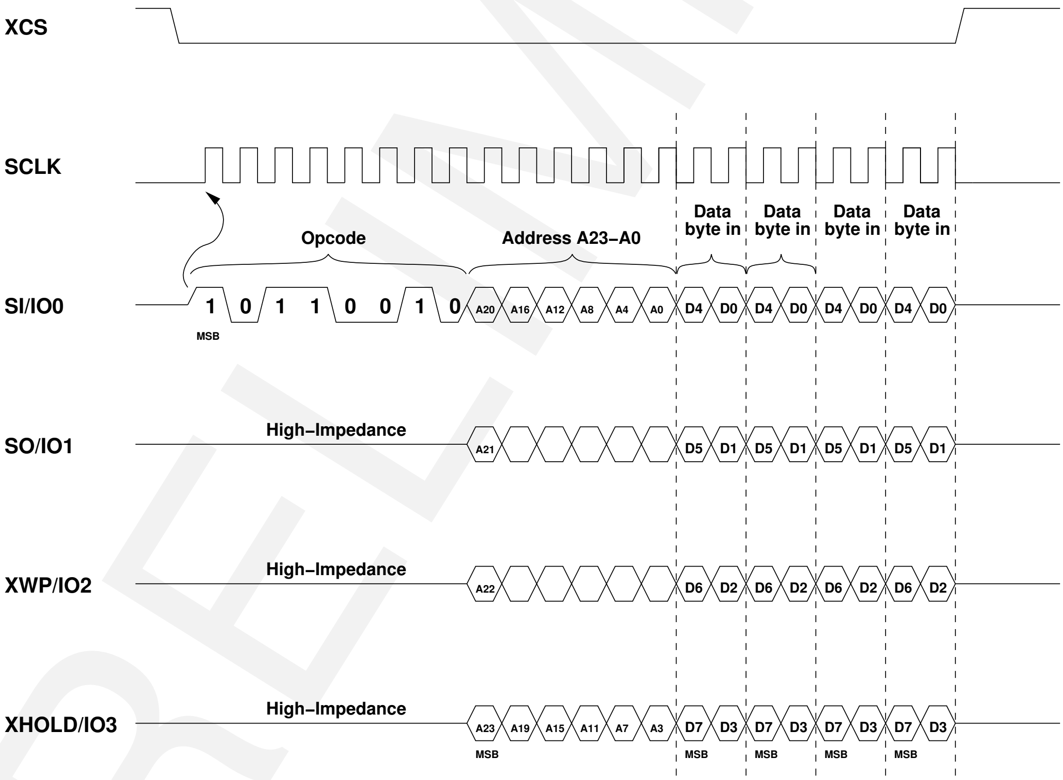


Figure 27: SPI Quad-Input, Quad Address Write

7.3 SPI Miscellaneous Commands

7.3.1 Read Status Register (05h)

The Read Status command is started by asserting XCS pin. After that the host controller sends the opcode, 05h. The device responds by clocking out a byte wide value of Status register. When XCS pin is deasserted, the clocking out of the register is ended and SO pin goes to high-impedance state.

Output Bits	Name		Type	Description	
7-6	StSPIMn	SPI Mode	RW	0 0 0 1 1 0 1 1	Word Mode (Default) Sequential Mode Page Mode Reserved
5	Reserved	Reserved	RW	0	Default
4	Reserved	Reserved	RW	0	Default
3-1	StUsern	User Bits	RW		User Bits
0	StSPIH	SPI Hold Function	RW	0 1	Hold (Default) No Hold

StSPIMn These bits indicate the operating mode of the SPI of the VS23S010D-S. StSPIMn bits affect the operation in all SPI SRAM read and write modes.

Reserved This bit is reserved. It has to be low always for correct functionality of the VS23S010D-S.

StUsern StUsern bits are user assignable and have no effect to operation on VS23S010D-S. Default value is low.

StSPIH StSPIH enables Hold functionality in Single and Dual mode SPI operations. Default value is "0" which means that Hold functionality is enabled.

7.3.2 Write Status Register (01h)

To write the GPIO Control register XCS pin must be first asserted and opcode 01h clocked into the device. After that byte-wide value is clocked in the device via SI pin. The value is input MSB (bit 7) first. The state of the Status Register bits is changed according to the received byte after the SCLK goes low. Note, that bit 5 has to be low always.

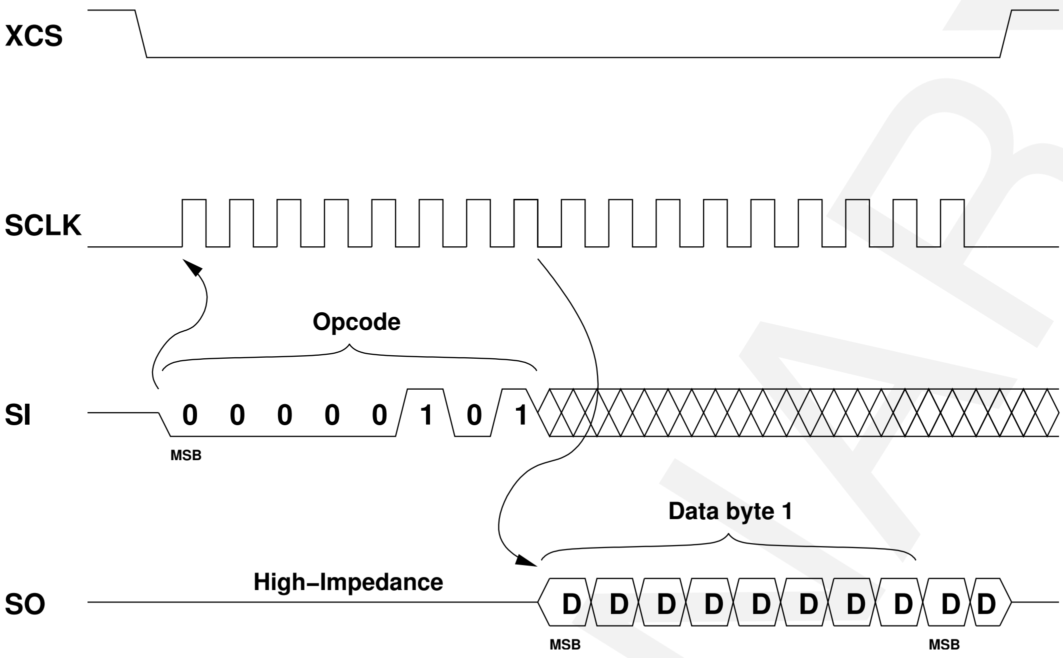


Figure 28: SPI Read Status Register

Write Status Register Format							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
StSPIM1	StSPIM0	Reserved, "0"	Reserved, "0"	StUser2	StUser1	StUser0	StSPIH

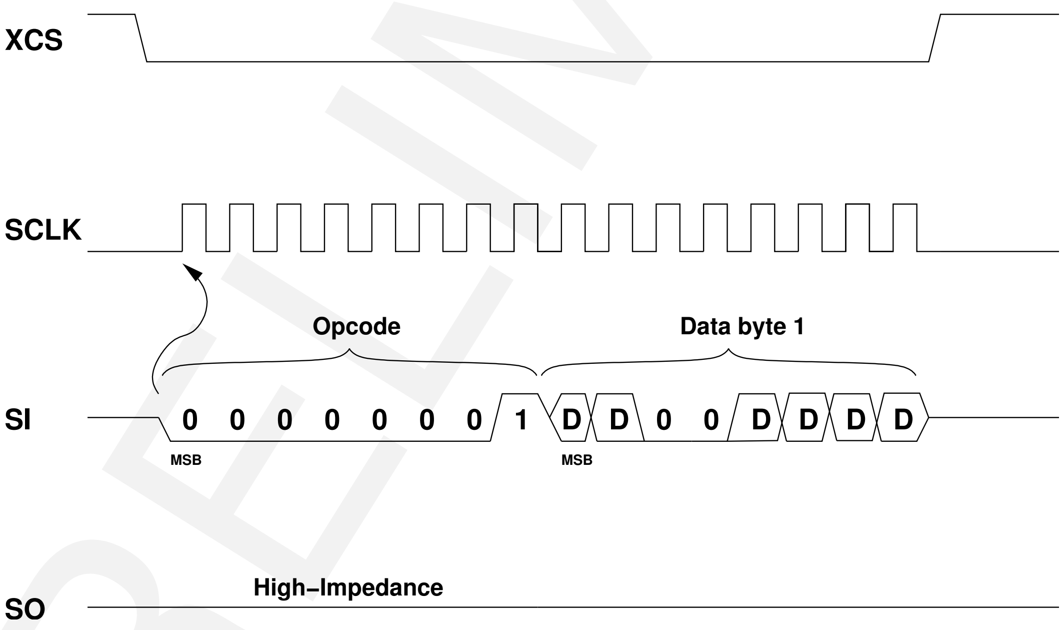


Figure 29: SPI Write Status Register

7.3.3 Read Manufacturer and Device ID (9Fh)

The Read Manufacturer and Device ID command is started by asserting XCS pin. After that the host controller sends the opcode, 9Fh. The device responds by clocking out a byte wide constant, value 2Bh. When XCS pin is deasserted, the clocking out of the data is ended and SO pin goes to high-impedance state.

Note, Manufacturer and Device ID is read-only register.

Bits	Name		Type	Description	
7-0	ID	Manufacturer and Device ID	R	2Bh	ID (default)

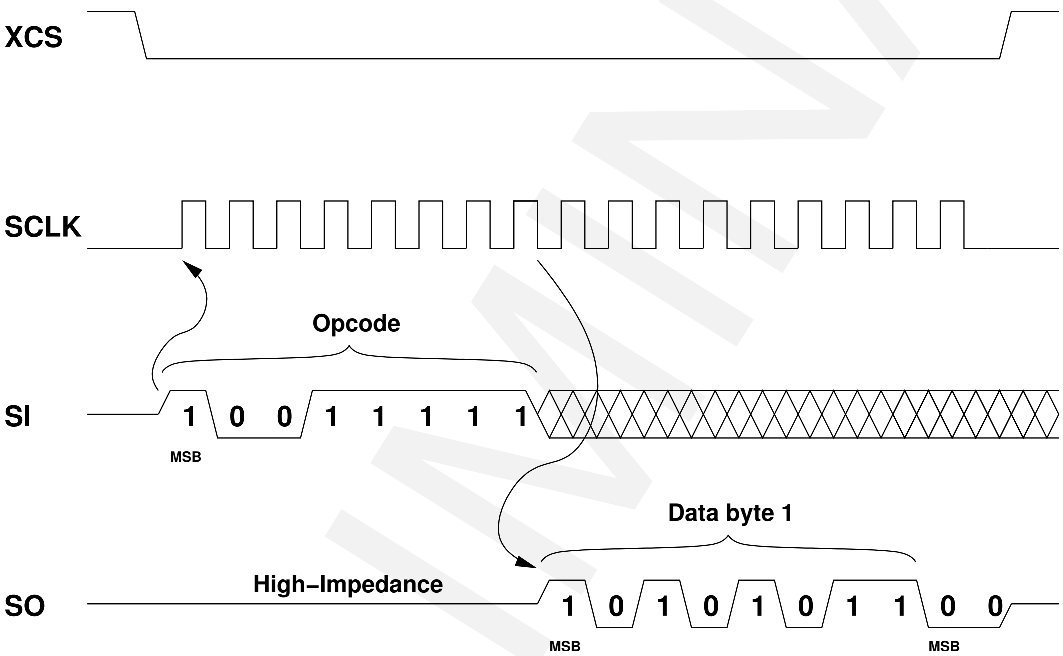


Figure 30: SPI Read Manufacturer and Device ID

8 Errata

Below are described situations in which VS23S010D-S devices with date-code 1441 and 1519 behave differently than expected. VLSI Solution Oy has corrected these issues for current devices.

8.1 Powering Up

Depending on the rise time of VCC pin, the ambient temperature and the final level of VCC pin the startup of the VS23S010D-S can take relatively long time.

Typically when rise time of VCC is fast, the final VCC level is above 1.75 V and operating temperature is not much below room temperature, the VS23S010D-S is fully operational in 20 ms after power-up. However, if the slope of VCC is slow, the final level is below 1.7 V and the ambient temperature is near the lowest allowed, the powering up can take several seconds.

8.2 Idle Current

Typically when VS23S010D-S is in idle state the VCC current is below 100 μA. Sometimes the idle current of VS23S010D-S can be up to 300 μA after power-up.

There is a simple method for lowering the excess idle current. This can be done by making the following SPI operations five times. The SPI sequence for lowering idle current is as follows:

- Send a SPI command 2Bh and after that 1000h as data in single I/O mode.
- Send a SPI command 2Bh and after that 0000h as data in single I/O mode.
- Repeat the above sequence five times.

8.3 Slow Data Interface Clock Slope

If slope of a VS23S010D-S data interface clock (SCLK) is very slow (over 20 ns) then there may occur data errors when data is read from VS23S010D-S. The probability of this issue depends on data values and the used board design (crosstalk of signals and stability of power supply of VS23S010D-S).

9 Document Version Changes

This chapter describes the most important changes to this document.

Version 0.93, 2016-12-19

- Fixed a typo.

Version 0.92, 2016-12-13

- Changed and updated Chapter 3

Version 0.91, 2015-05-07

- Changed and updated Chapter 3
- Added Chapter 8.3

Version 0.9, 2015-01-16

- Reorganized Chapter 3

Version 0.8, 2015-01-09

- Pull-up resistors in XWP/IO2 and XHOLD/IO3 pins
- Multi-bit address SPI modes
- Manufacturer and device ID changed.

Version 0.7, 2013-05-30

- Added SPI Word, Page and Sequential modes.
- Added Status register write.
- New packages and pin-outs

Version 0.6, 2012-06-14

- Updated clock frequency and power consumption information.
- Reorganized document according to functionality.

Version 0.5, 2012-02-03

- Added information for SOIC16 package.

10 Contact Information

VLSI Solution Oy
Entrance G, 2nd floor
Hermiankatu 8
FI-33720 Tampere
FINLAND

URL: http://www.vlsi.fi/
Phone: +358-50-462-3200
Commercial e-mail: sales@vlsi.fi

For technical support or suggestions regarding this document, please participate at
http://www.vsdsp-forum.com/
For confidential technical discussions, contact
support@vlsi.fi