VS10XX AppNote: VS1002 to VS1033 migration checklist

Description

This document describes how to migrate from VS1002 to VS1033. This document lists hardware and software differencies and other considerations.

This document applies to all versions of VS1002 and VS1033.

Revision History			
Rev	**Date**	**Author**	**Description**
1.00	2006-04-07	PLe	Initial revision.

Table of Contents

1 General

VS1033 has many updated features compared to VS1002. The most significant updates are WMA and AAC support, MIDI support, Internal PLL, Line-input for recording, Separate voltage input for VSDSP core and 4 additional GPIO pins.

A stripped down version of VS1033 is also available. This version does not have WMA or AAC support. All other features are supported. This version is intended to replace VS1002 in applications where WMA and AAC is not reguired.

Due to these new features the pinout and register interface has also changed.

2 Hardware

VS1002 and VS1033 have few differecies in hardware.

2.1 Core Voltage

The biggest difference is the Core Voltage in VS1033. In addition to Analog and Digital (IO) Voltage the VS1033 features a separate voltage input for the VSDSP core. This voltage can be in the range of 2.4V .. 2.7V. The recommended value is 2.5V.

The simplest solution is to use a forward diode from IOVDD to CVDD. This solution can however cause unwanted transients at the analog outputs during power-up and power-down. It is recommended to use a linear regulator with suffecent filtering to feed the CVDD. Also, each CVDD pin should be bypassed with 100nF capasitors.

2.2 GPIO pins

VS1033 has four additional GPIO pins. These pins should be treated as in VS1002. If not used they should be tied to ground through 100kOhm resistor. All GPIO pins are input after power-up. When not used all GPIO pins can be tied together and grounded with a single 100k resistor.

2.3 Internal PLL

VS1033 has an internal PLL that can be used to generate higher internal clock to provide sufficent internal clock speed for WMA and AAC decoding. See more info

on PLL and the CLOCKF register from VS1033 datasheet chapter 8.6.4.

VS1033 has a VCO output pin. This pin is used for tests only and should be left unconnected.

2.4 Line Input

In addition to microphone input the VS1033 also features a line-level input. This input can be used to record ADPCM audio. Line input can be selected from SCI_MODE register.

2.5 LQFP-48 and BGA-49 Pin Descriptions

The following table describes the new pins and functions for VS1033.

See dimensions for BGA and LQFP packages from "www.vlsi.fi"

Both LPQFP-48 and BGA-49 are lead (Pb) free and also RoHS compliant packages. RoHS is a short name of *Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment.*

Pin descriptions:

Pin Name	LQFP Pin	BGA Ball	Pin Type	New Function For VS1033
MICP	1	C3	AI	
MICN	2	C2	AI	
XRESET	3	B1	DI	
DGND0	4	D2	DGND	
CVDD0	5	C1	CPWR	Core power supply
IOVDD0	6	D3	IOPWR	
CVDD1	7	D1	CPWR	Core power supply
DREQ	8	E2	DO	
GPIO2 / DCLK[1]	9	E1	DIO	
GPIO3 / SDATA[1]	10	F2	DIO	
GPIO6	11	F1	DIO	General purpose IO 6
GPIO7	12	G1	DIO	General purpose IO 7
XDCS / BSYNC[1]	13	E3	DI	
IOVDD1	14	F3	IOPWR	
VCO	15	G2	DO	
DGND1	16	F4	DGND	
XTALO	17	G3	AO	
XTALI	18	E4	AI	
IOVDD2	19	G4	IOPWR	
IOVDD3		F5	IOPWR	
DGND2	20		DGND	
DGND3	21	G5	DGND	
DGND4	22	F6	DGND	
XCS	23	G6	DI	
CVDD2	24	G7	CPWR	Core power supply
GPIO5 / I2S_MCLK[3]	25	E5	DIO	General purpose IO 5 / I2S_MCLK
RX	26	E6	DI	
TX	27	F7	DO	
SCLK	28	D6	DI	
SI	29	E7	DI	
SO	30	D5	DO3	
CVDD3	31	D7	CPWR	Core power supply
TEST	32	C6	DI	
GPIO0 / I2S_SCLK[3]	33	C7	DIO	
GPIO1 / I2S_SDATA[3]	34	B6	DIO	
GND	35	B7	DGND	
GPIO4 / I2S_LROUT[3]	36	A7	DIO	General purpose IO 4 / I2S_LROUT
AGND0	37	C5	APWR	
AVDD0	38	B5	APWR	
RIGHT	39	A6	AO	
AGND1	40	B4	APWR	
AGND2	41	A5	APWR	
GBUF	42	C4	AO	
AVDD1	43	A4	APWR	
RCAP	44	B3	AIO	
AVDD2	45	A3	APWR	
LEFT	46	B2	AO	
AGND3	47	A2	APWR	
LINEIN	48	A1	AI	Line Input

Pin types:

Type	Description
DI	Digital input, CMOS Input Pad
DO	Digital output, CMOS Input Pad
DIO	Digital input/output
DO3	Digital output, CMOS Tri-stated Output Pad
AI	Analog input

Type	Description
AO	Analog output
AIO	Analog input/output
APWR	Analog power supply pin
DGND	Core or I/O ground pin
CPWR	Core power supply pin
IOPWR	I/O power supply pin

3 Application Considerations

This chapter gives general info on applications using VS1033.

3.1 Hardware Design

RC-snubbers described in "http://www.vlsi.fi/appnotes/vs10XXan_output.pdf" must be connected to LEFT, RIGHT and GBUF even if GBUF is not used. RC-pairs should be connected righ after the output jack. If line-out connection is used RC-pairs must be connected right after VS1033 analog outputs with no components between RC-pairs and VS1033.

PCB traces from analog connections (including mic and line) should be kept as short as possible.

Each voltage input pin should be bypassed with 100nF capasitor for best performance.

Ground plane should be used under the VS1033. Each ground pin should be connected to this plane as close to the chip as possible.

3.2 Software Considerations

Fast Forward and Rewind operations differ forbetween different audio formats. MP3 is well suited for random access and can be fast forwarded and rewing as in VS1002. WMA, AAC, Midi and WAV need special attention. Use HDAT1 register to determine the current playing file type. See VS1033 datasheet chapter 9.9 for detailed info.

VS1033 has a set of extra parameters to give the user additional control over the chips functions. For example fast forward and rewind for WMA and AAC is supported by new hardware features. See datasheet chapter 9.8 for more info.

4 SCI Registers

VS1002 and VS1033 have few differencies in registers that are not compatible with each other. Extreme care should be taken when porting VS1002 software to VS1033. The following chapters list these differencies. See more info from VS1002 and VS1033 datasheets.

4.1 MODE

SM_SETTOZERO changed to SM_LAYER12. Set to 1 to allow MPEG layers 1 and 2. Notice that this may require a separate decoder licence not included in the chip price.

SM_PLUSV changed to SM_SETTOZERO2. Set to zero and forget.

New bits:

SM_LINEIN, set to one to select line input instead of mic for recording.

SM_CLK_RANGE, if set to one, divides input clock by two. Set to zero for 12 .. 13MHz clock, one for 24 .. 26 MHz clock

4.2 STATUS

SS_VER is 5 for VS1033

4.3 BASS

While VS1002 had only bass control VS1033 has bass and treble controls. VS1002 Bass controll is compatible with the new register.

See more info from VS1033 datasheet chapter 8.6.3

4.4 CLOCKF

CLOCKF has had some major changes since VS1002. It now controls the internal PLL of the VS1033 and must be set accordingly. See more info from VS1033 datasheet chapter 8.6.4.

4.5 WRAMADDR

New adresses for GPIO pins. Also the adresses for X, Y and I RAM have changed.

4.6 HDAT0 and HDAT1

These registers give info on the supported audio formats. With the new codec supported in VS1033 these registers contain new info.

5 User Applications

Because the memory adresses have changed the User Apps written for VS1002 must be ported to VS1033. See new memory map and other info on VS1033 registers and functions from VS1033 datasheet chapter 10.

6 Document Version Changes

This chapter describes the most important changes to this document.

Version 1.00, 2006-04-07

- Initial version.

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Note: If you have questions, first see
http://www.vlsi.fi/vs1001/faq/
http://www.vlsi.fi/vs1011/faq/
http://www.vlsi.fi/vs1002/faq/
http://www.vlsi.fi/vs1003/faq/
http://www.vlsi.fi/appnotes