VS1001 TO VS1011 MIGRATION CHECKLIST

REQUIRED CONSIDERATIONS

BSYNC pin
• If BSYNC is generated properly, it is no need to change it for VS1011.
• If BSYNC was earlier tied to VCC, it is needed to generate one BSYNC transition from low to high at least 10 us after rising edge of RESET signal. (You can connect RESET signal to BSYNC via series resistor followed by capacitor.)
• It is recommend to use the NEW_MODE (BSYNC as xDCS) or generate BSYNC clock.

User RAM code functions
• Firmware functions (e.g. Loudness etc.) and user specific features written for VS1001 need to be modified.
• Download and use functions specifically written for VS1011.
• Check if the required function is already available in ROM of VS1011 (see datasheet and application notes).

SDI Master Mode
• There is no Master Mode in VS1011.

GPIO pins
• All unused GPIO pins should be tied low with a 10K...100K resistor.
• GPIO0 should always be tied low. If other GPIO pins are left floating, it will not cause damage but can cause additional power consumption.

SCI pins
• In VS1001 the SO pin is three-stated until the start of SO data transmission.
• In VS1011 a low level at xCS turns the SO pin driver active. The pin is driven low until start of transmission. The actual transmission is just as in VS1001.
• See VS1011 datasheet figure 5: SCI Word Read.

RECOMMENDED IMPROVEMENTS

Minimizing power consumption
• VS1011 operates from lower voltage than VS1001.
• Schottky diode can be used to lower the voltage of DVDD in case regulator voltage can not be changed.
• For example BAT54C Schottky diode lowers DVDD from 2.8V to 2.35V reducing the power consumption by 5 milliamperes at Fclk = 28.632MHz (14.318Mhz x 2). You can still use the 2.8V for I/O signals.

Clock rates
• Observe the same concerns between master clock and maximum decoded bitrate as discussed in VS1001 Application Notes.
• VS1011 is capable to operate at much higher clock frequencies than VS1001. This advantage can be used either to decrease DVDD or add more user specific processing.